

Starload Schematics

Skylake-U

2016-02-18

REV : A00



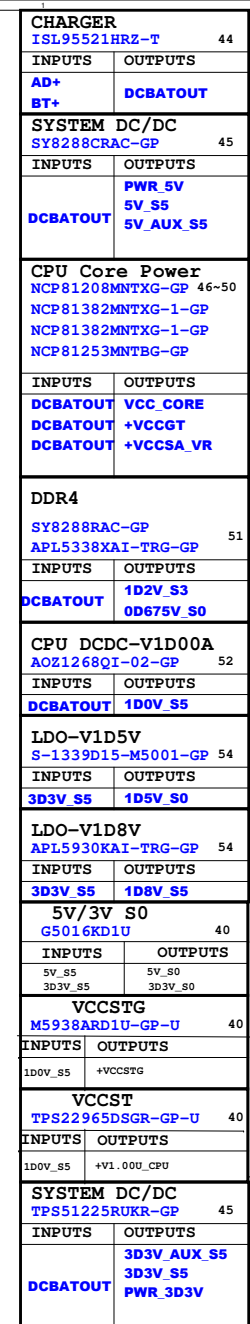
DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

<Variant Name>		
DELL		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Cover Page		
Size A3	Document Number Starload SKL-U	Rev A00
Date: Thursday, February 18, 2016 Sheet 1 of 106		

Star lord SKL-U Block Diagram




Main Func = CPU

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Title

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Size

A3

Document Number

Starload SKL-U

Rev

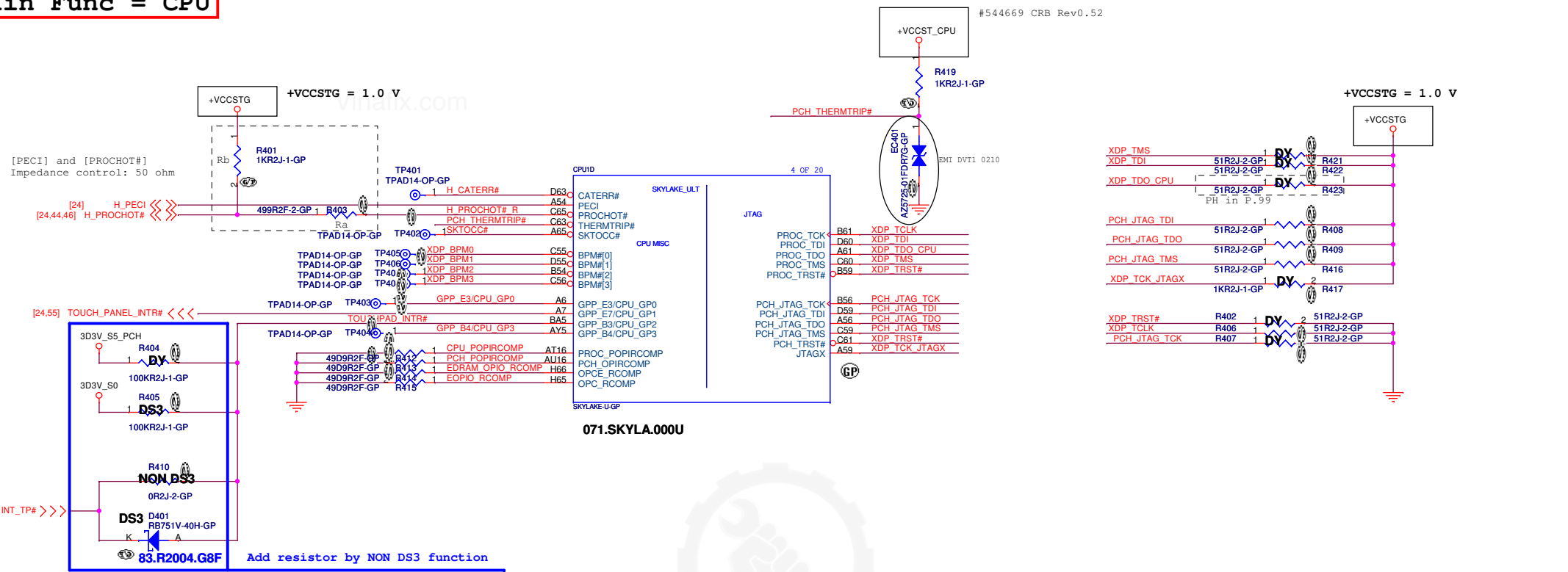
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Date: Thursday, February 18, 2016

Sheet 3 of 106

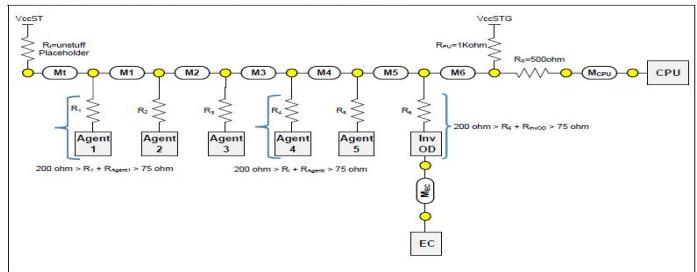
Main Func = CPU

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

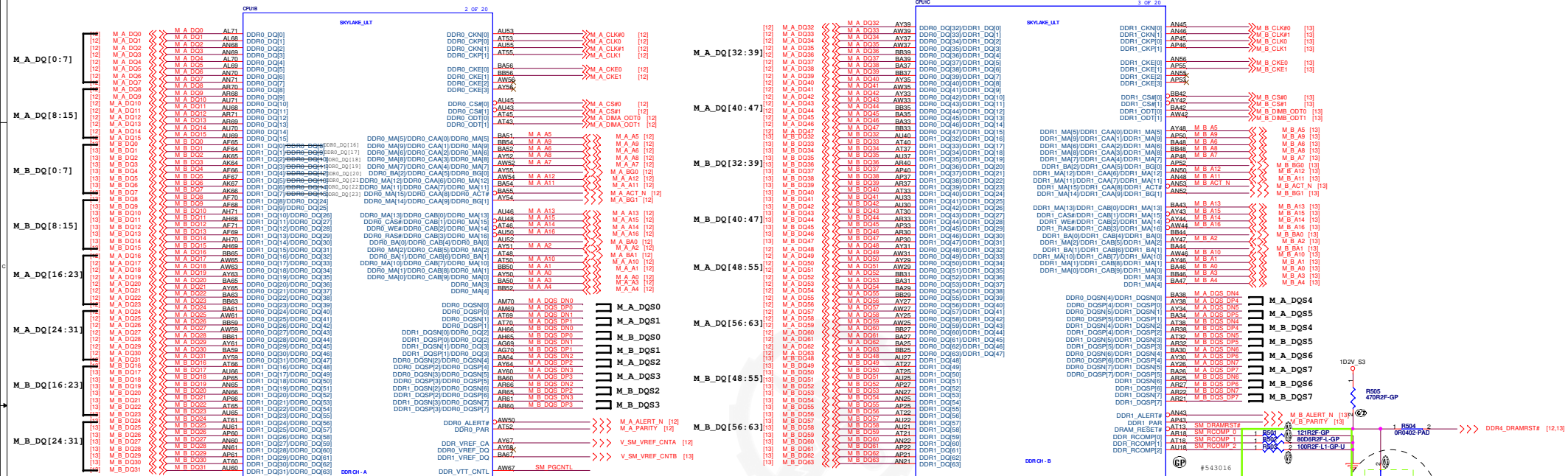


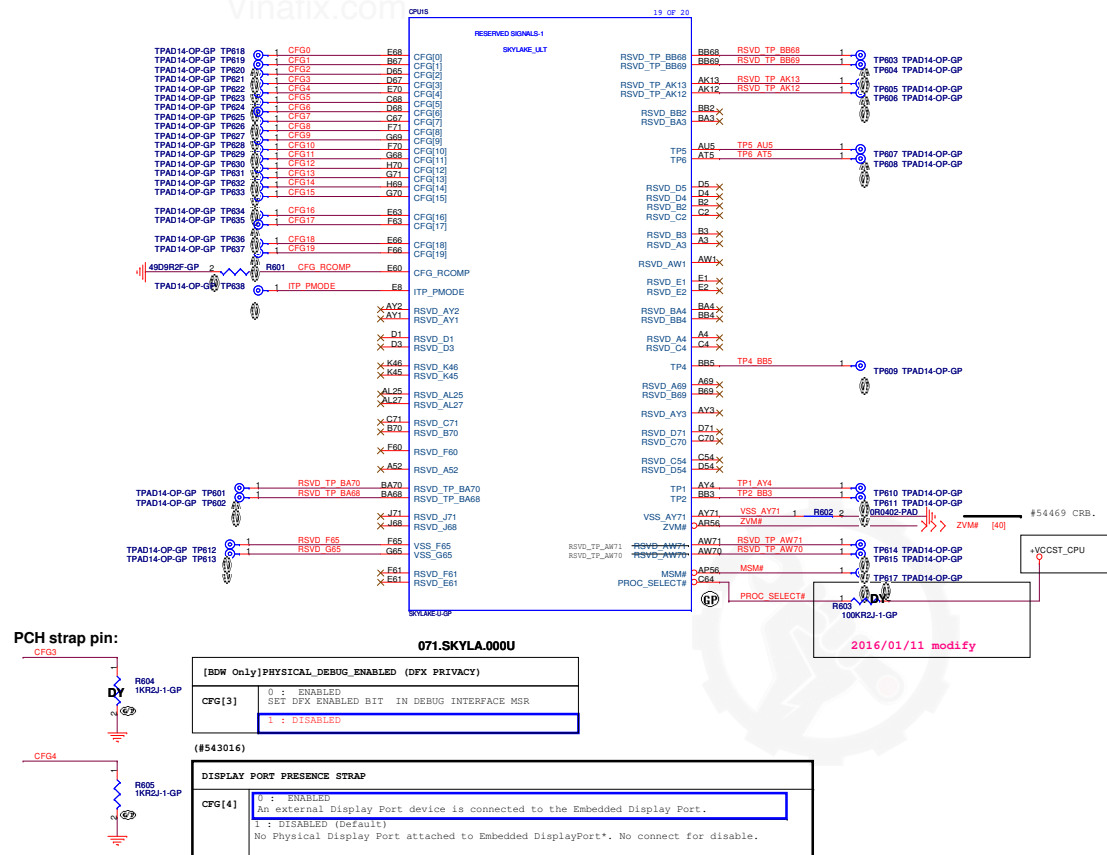
(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology

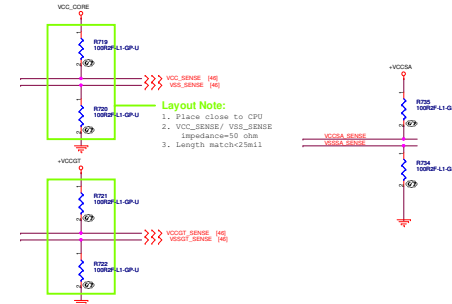
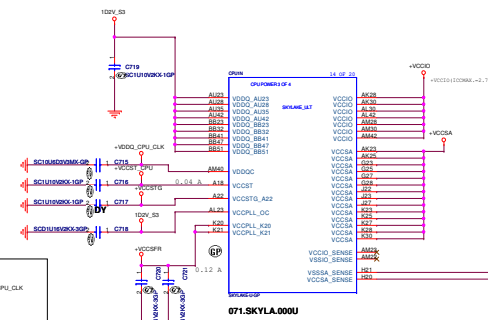
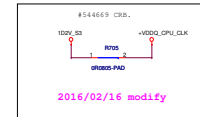
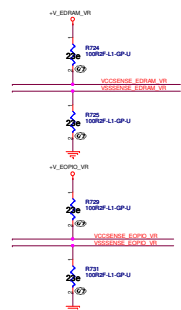
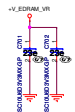
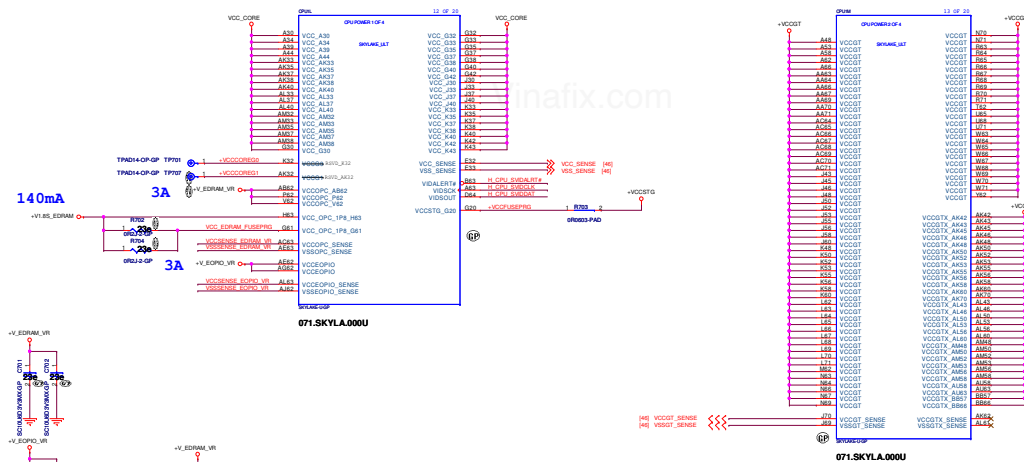


M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route (M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches





```
SKL(#543016) :
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*
```

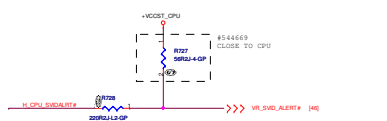
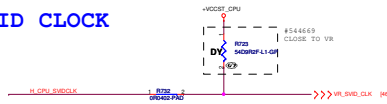


SVID DATA

Layout Note:
The total length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.



SVID CLOCK



SVID_543016:

Figure 10-7. Routing Illustration for SVID Topology

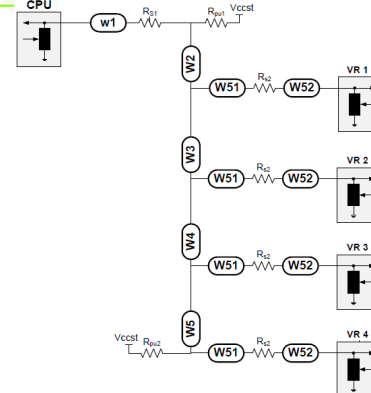


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W1 [inches]	W2 [inches]	R _{DS(on)} [Ω]	R _{DS(on)} [Ω]	R _{DS(on)} [Ω]	R _{DS(on)} [Ω]	V _{CE(sat)} [V]
VIDSOUT							100	100	0	10	
VIDSCK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.0
VIDALERT							56	Empty	220	0	

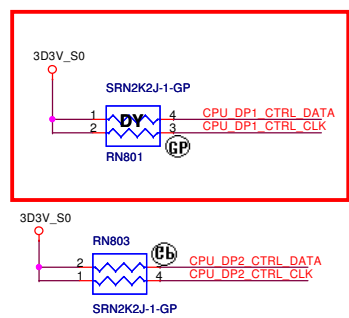
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Starload SKL-U
CPU(VCC CORE)
Document Number: A00
Revision: 1.0
Date: 2016/02/16

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Dummy, Vendor suggest
20141117

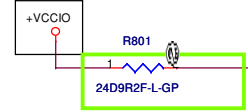


HDMI

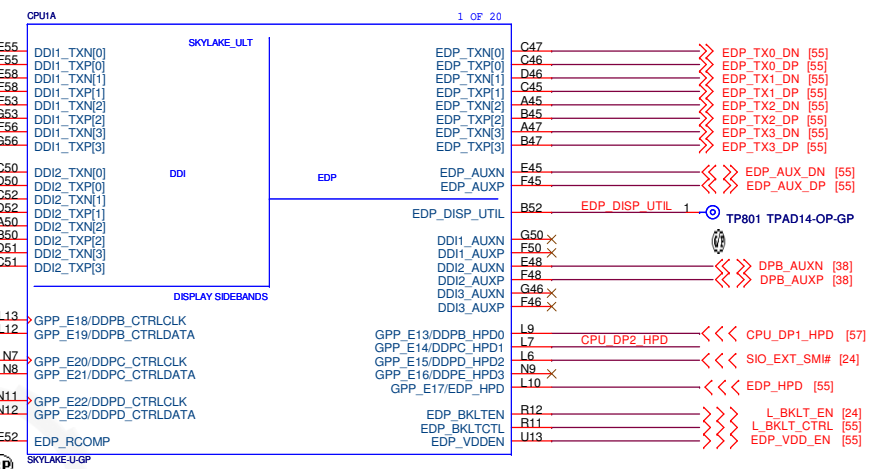
DP and DP to VGA

HDMI

Check



- [57] HDMI_DATA2#
- [57] HDMI_DATA2
- [57] HDMI_DATA1#
- [57] HDMI_DATA1
- [57] HDMI_DATA0#
- [57] HDMI_DATA0
- [57] HDMI_CLK#
- [57] HDMI_CLK
- [38] PCH_DPC_N0
- [38] PCH_DPC_P0
- [38] PCH_DPC_N1
- [38] PCH_DPC_P1
- [38] PCH_DPC_N2
- [38] PCH_DPC_P2
- [38] PCH_DPC_N3
- [38] PCH_DPC_P3



071.SKYLA.000U

(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

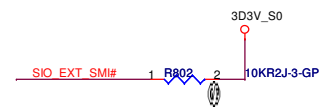
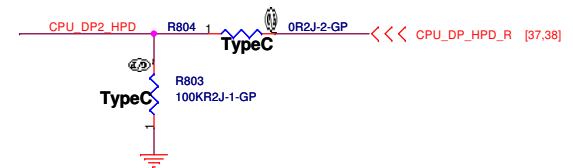
(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω \pm 1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 Ω resistor.



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Title: **CPU (DISPLAY)**

Size: A3 Document Number: **Starload SKL-U** Rev: **A00**

Date: Thursday, February 25, 2016 Sheet 8 of 106

Main Func = CPU

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CORE

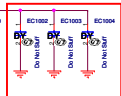
20140814 DAVID

U-line 23e 28W
IccMax current-10ms max = 34 A

220 0603 x 35 (5 DT)



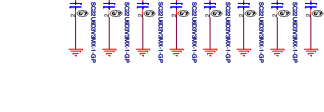
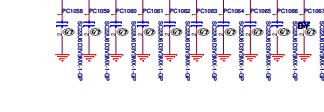
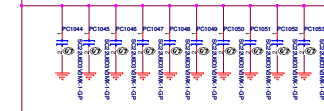
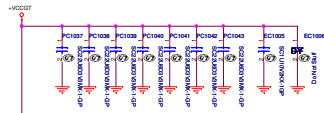
SMT case, 20141118



SLICED GT

U-line 23e 28W
IccMax current-10ms max[A] = 67 A

220 0603 x35 (5 DT)



VCCSA

220 0603 x13 (5 DT)



011/10/16 modify (Power team request)

Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (04.5mD ESR)	Placed at primary side near to VR output
VCCGT Power Plane at VR output	1x 220uF (04.5mD ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (04.5mD ESR)	Placed at primary side near to VR output
VCCGTx Power Plane at VR output	1x 220uF (04.5mD ESR)	Placed at primary side near to VR output
VCCIO Power Plane at VR output	2x 47uF 0805	Additional components needed when supporting 23e
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

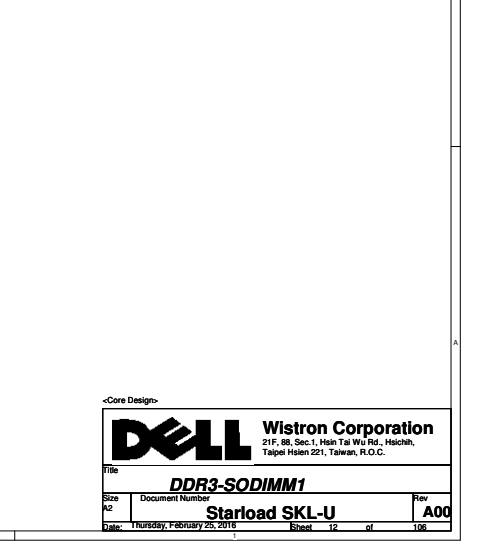
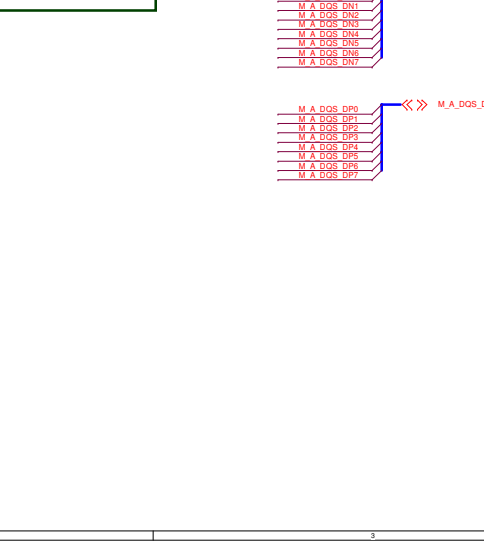
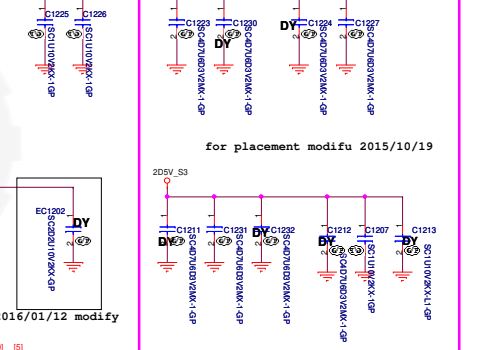
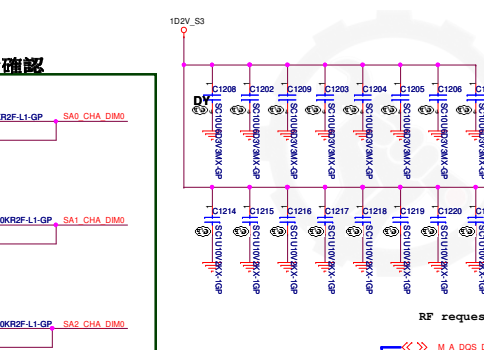
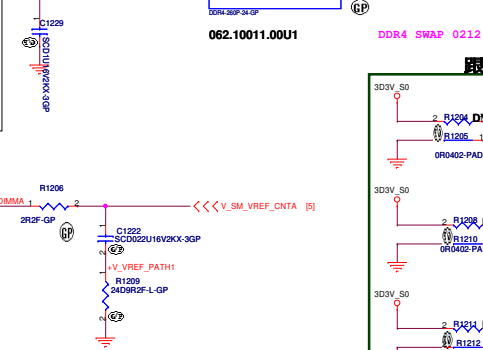
Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V)	Place as close to the package as possible
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Additional components needed when supporting 23e
		5x 22uF 0603	
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package
			Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
VDDQ	2x 10uF 0402		Place as close to the package as possible
	4x 1uF 0201		
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPL	1x 1uF 0402		Place as close to the package as possible
VCCST	1x 1uF 0402		Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package
VCCSTG			Placeholder only
VCCSTG	2x 10uF 0402		Place on secondary side, underneath the package
VCCSTG	1x 10uF 0402		Place on secondary side, underneath the package
VCCSTG	6x 1uF 0201		



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Title
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Size A4	Document Number Starload SKL-U	Rev A00
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Date: Thursday, February 18, 2016 Sheet 14 of 106

Main Func = PCH

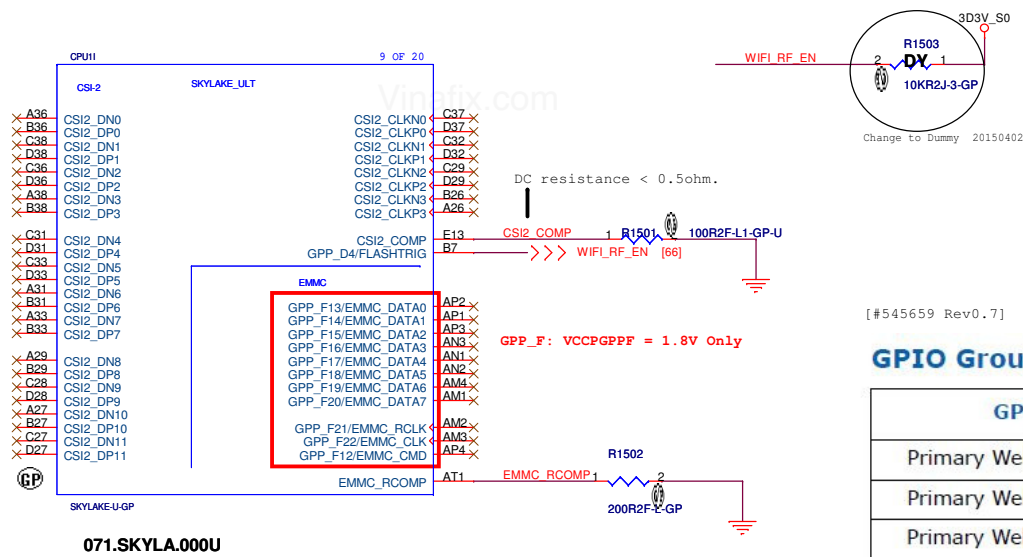


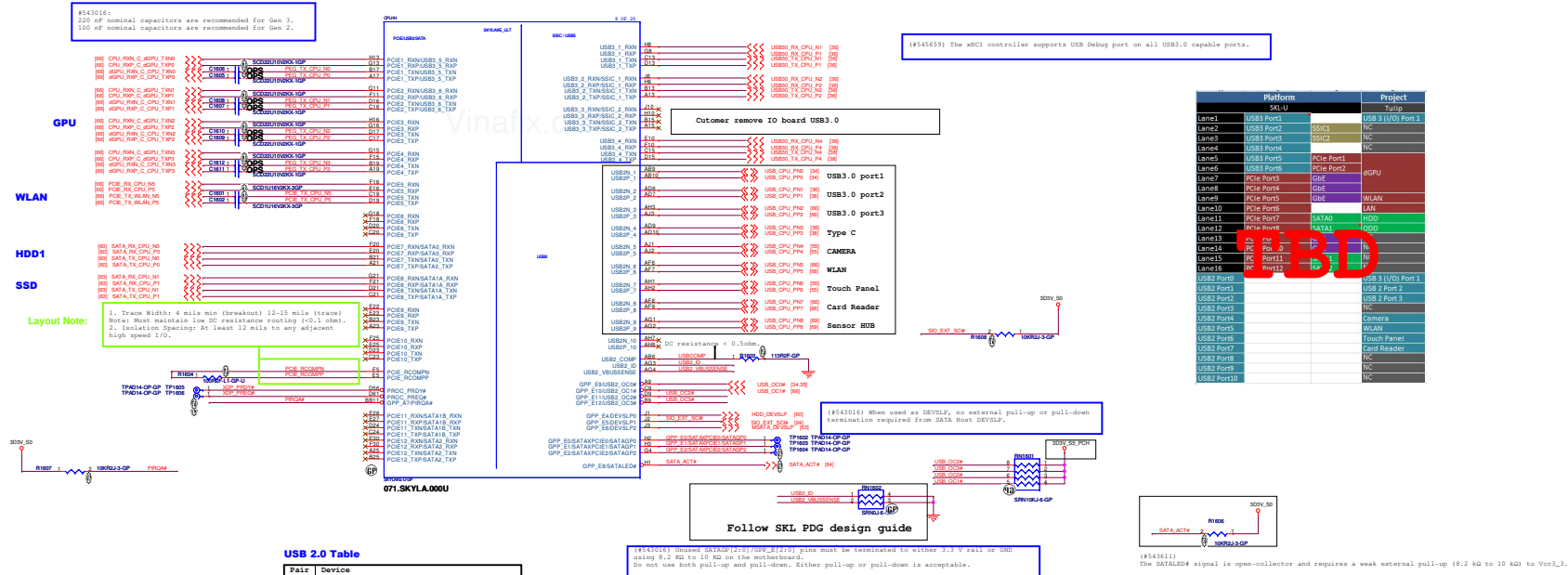
Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSENT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V



Platform	SKL-U	Project
Lane1	USB3 Port1	Tulip
Lane2	USB3 Port2	SSIC
Lane3	USB3 Port3	SSIC
Lane4	USB3 Port4	NC
Lane5	USB3 Port5	SSIC
Lane6	USB3 Port6	SSIC
Lane7	PCIe Port3	SSIC
Lane8	USB3 Port7	SSIC
Lane9	PCIe Port4	SSIC
Lane10	PCIe Port5	SSIC
Lane11	PCIe Port6	SSIC
Lane12	PCIe Port7	SSIC
Lane13	PCIe Port8	SSIC
Lane14	PCIe Port9	SSIC
Lane15	PCIe Port10	SSIC
Lane16	PCIe Port11	SSIC
Lane17	PCIe Port12	SSIC
Lane18	PCIe Port13	SSIC
Lane19	PCIe Port14	SSIC
Lane20	PCIe Port15	SSIC
Lane21	PCIe Port16	SSIC
Lane22	PCIe Port17	SSIC
Lane23	PCIe Port18	SSIC
Lane24	PCIe Port19	SSIC
Lane25	PCIe Port20	SSIC
Lane26	PCIe Port21	SSIC
Lane27	PCIe Port22	SSIC
Lane28	PCIe Port23	SSIC
Lane29	PCIe Port24	SSIC
Lane30	PCIe Port25	SSIC
Lane31	PCIe Port26	SSIC
Lane32	PCIe Port27	SSIC
Lane33	PCIe Port28	SSIC
Lane34	PCIe Port29	SSIC
Lane35	PCIe Port30	SSIC
Lane36	PCIe Port31	SSIC
Lane37	PCIe Port32	SSIC
Lane38	PCIe Port33	SSIC
Lane39	PCIe Port34	SSIC
Lane40	PCIe Port35	SSIC
Lane41	PCIe Port36	SSIC
Lane42	PCIe Port37	SSIC
Lane43	PCIe Port38	SSIC
Lane44	PCIe Port39	SSIC
Lane45	PCIe Port40	SSIC
Lane46	PCIe Port41	SSIC
Lane47	PCIe Port42	SSIC
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Lane50	PCIe Port45	SSIC
Lane51	PCIe Port46	SSIC
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Lane61	PCIe Port56	SSIC
Lane62	PCIe Port57	SSIC
Lane63	PCIe Port58	SSIC
Lane64	PCIe Port59	SSIC
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Lane68	PCIe Port63	SSIC
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Lane73	PCIe Port68	SSIC
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Lane78	PCIe Port73	SSIC
Lane79	PCIe Port74	SSIC
Lane80	PCIe Port75	SSIC
Lane81	PCIe Port76	SSIC
Lane82	PCIe Port77	SSIC
Lane83	PCIe Port78	SSIC
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Lane85	PCIe Port80	SSIC
Lane86	PCIe Port81	SSIC
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Lane94	PCIe Port89	SSIC
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Lane96	PCIe Port91	SSIC
Lane97	PCIe Port92	SSIC
Lane98	PCIe Port93	SSIC
Lane99	PCIe Port94	SSIC
Lane100	PCIe Port95	SSIC
Lane101	PCIe Port96	SSIC
Lane102	PCIe Port97	SSIC
Lane103	PCIe Port98	SSIC
Lane104	PCIe Port99	SSIC
Lane105	PCIe Port100	SSIC

USB 2.0 Table

Port	Device
0	USB3.0 port1
1	USB3.0 Port2 (Debug Port/IOBD)
2	USB3.0 Port3 (IOBD)
3	Sensor HUB
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

Table 24-2. PCI Express* Port Feature Details

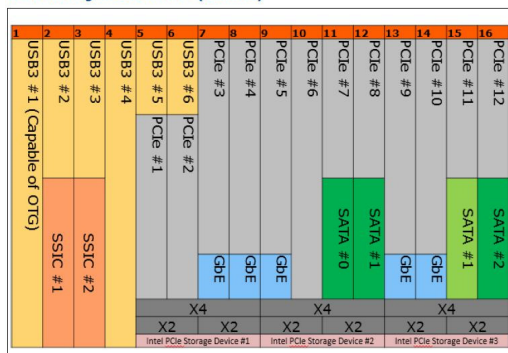
SKL	Max Devices (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Table 24-3. PCI Express* Link Configurations Supported

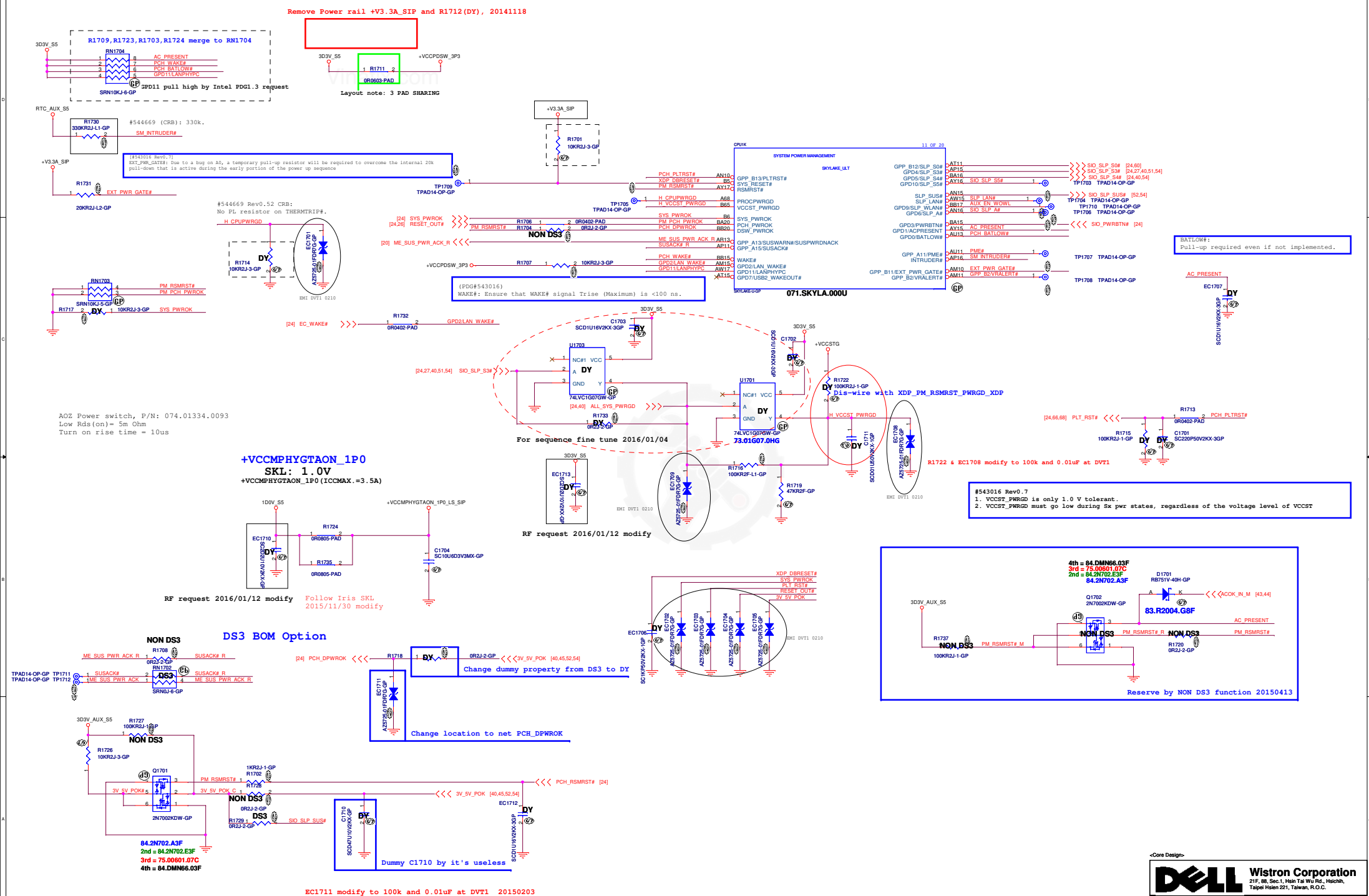
SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3		Port4		Port5		Port7		Port8	
	4x1	Port1		Port2		Port3		Port4		Port5		Port6	
	1x4	Port1				Port5				Port9			
Y	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3		Port4		Port5		Port7		Port8	
	4x1	Port1		Port2		Port3		Port4		Port5		Port6	
	1x2									Port9			
	2x1									Port9			

#545659 (SKL_PCH_U_XD0 Rev0.7)

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)



5
Main Func = PCH



PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

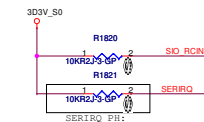
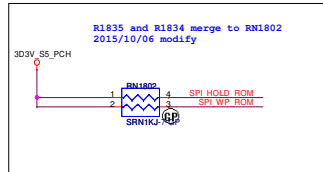
This signal has a weak internal pull-down.

PCH strap pin:

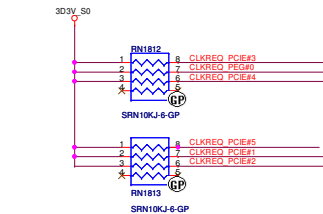
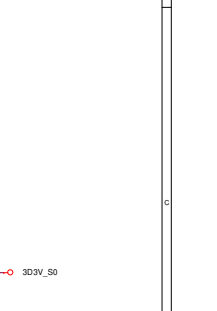
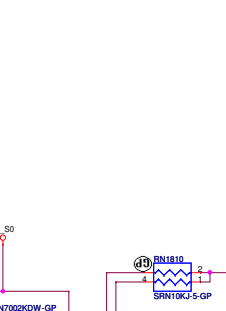
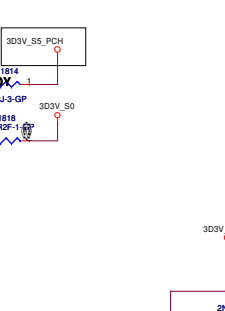
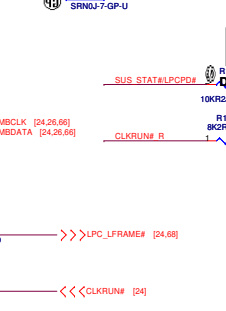
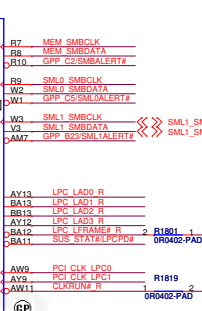
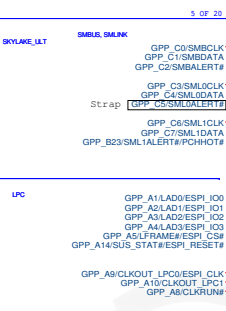
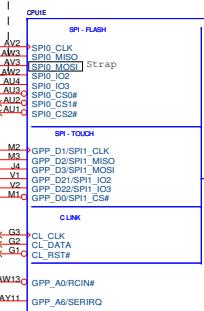
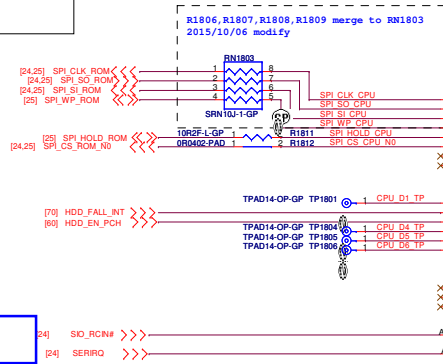
BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

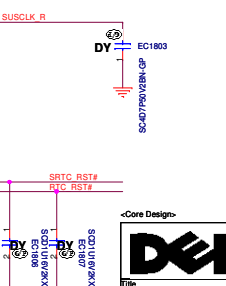
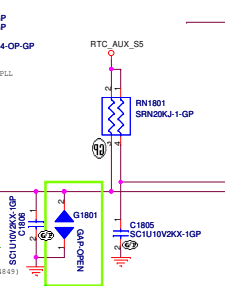
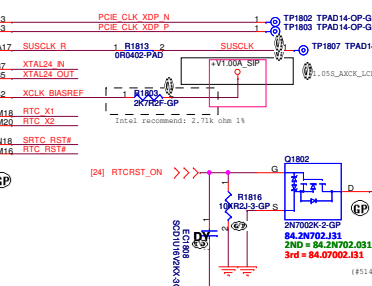
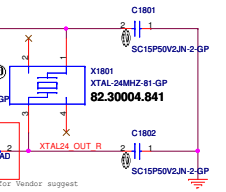
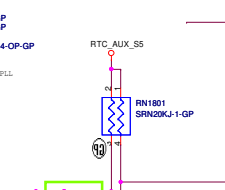
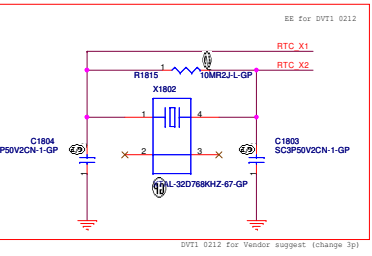
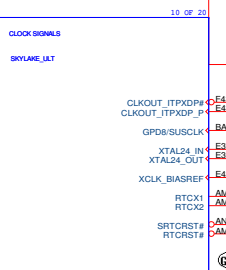
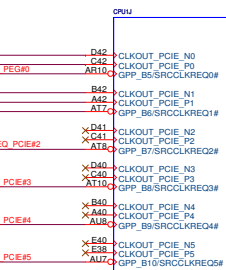
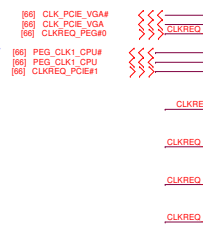
This signal has a weak internal pull-up



RCIN#:
Frequency to Avoid: 33 MHz



WLAN

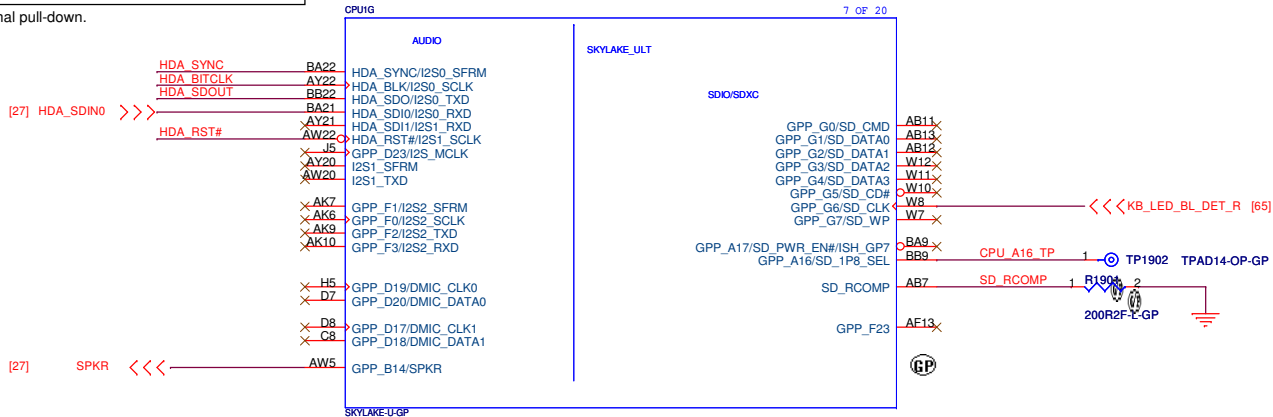


Main Func = PCH

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.



PCH strap pin:

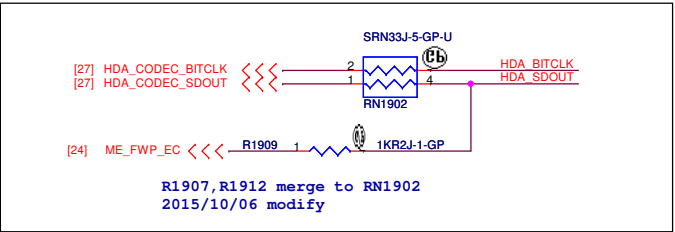
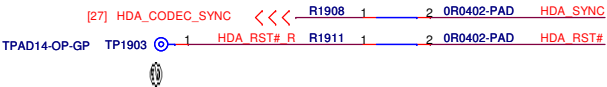
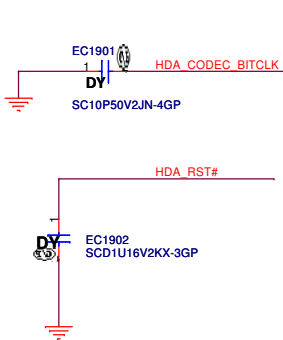
Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDO	Low = Default ★ High = Enable

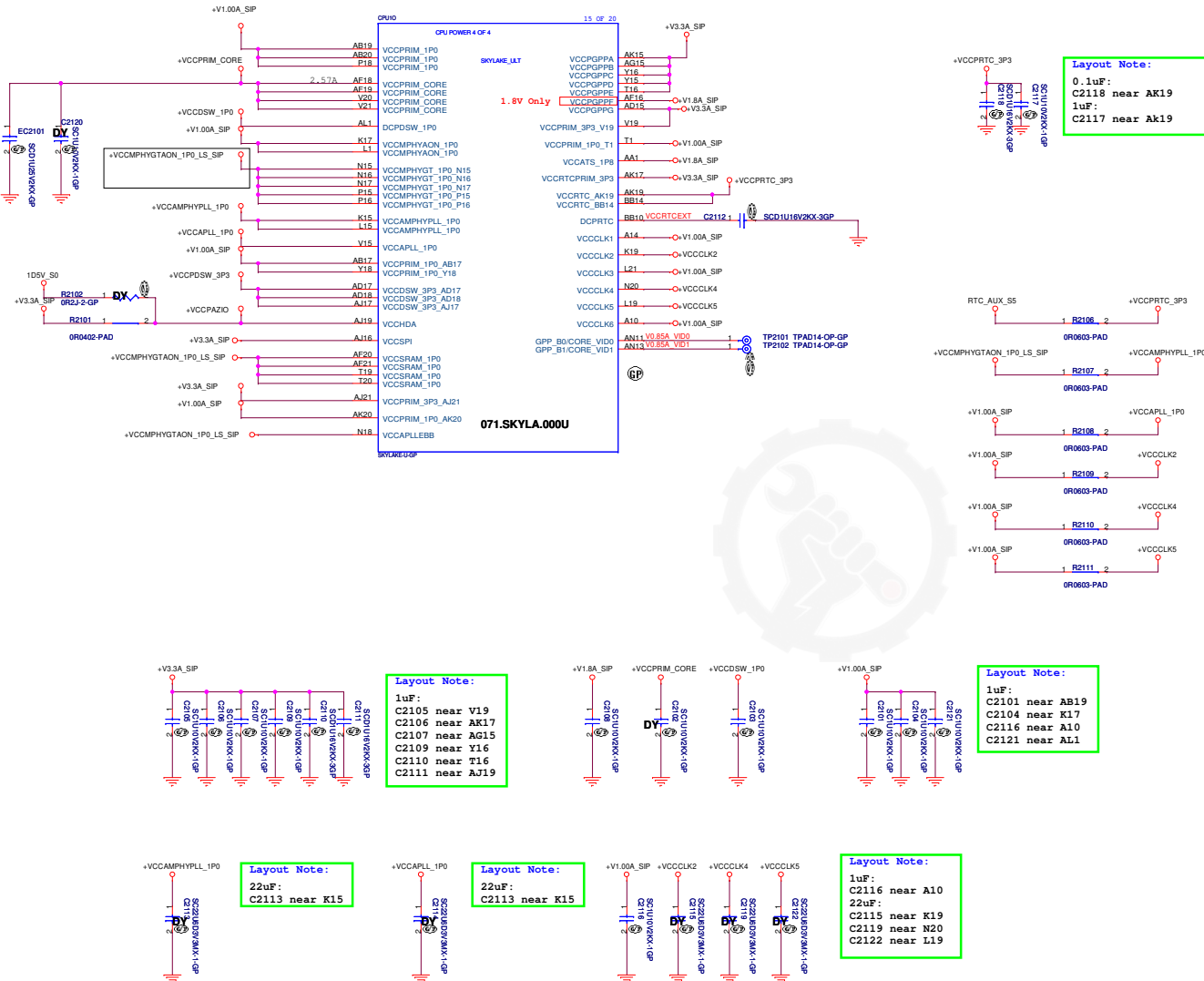
The internal pull-down is disabled after PLTRST# deasserts

PCH strap pin:

NO REBOOT	
HDA_SPKR	★ Low = Enable (Default) High = Disable

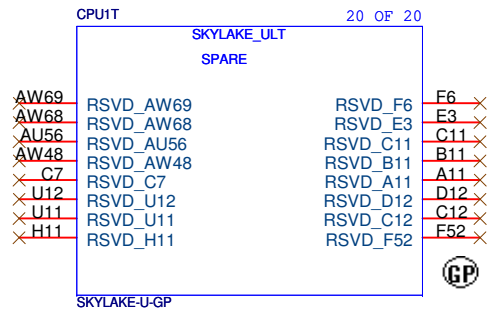
The internal pull-down is disabled after PLTRST# deasserts





Main Func = PCH

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071.SKYLA.000U



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Title

CPU (RSVD)

Size
A4

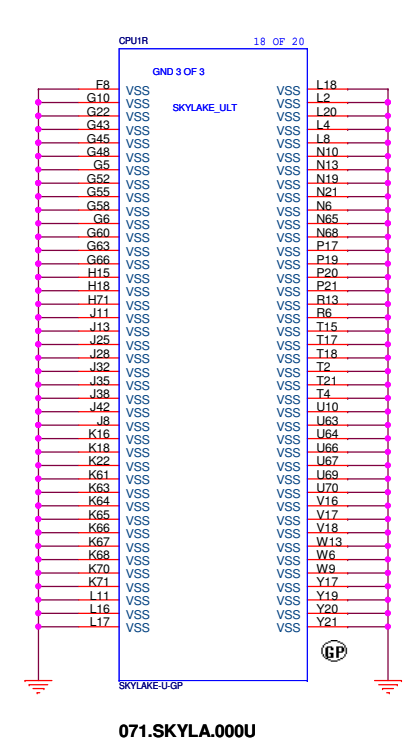
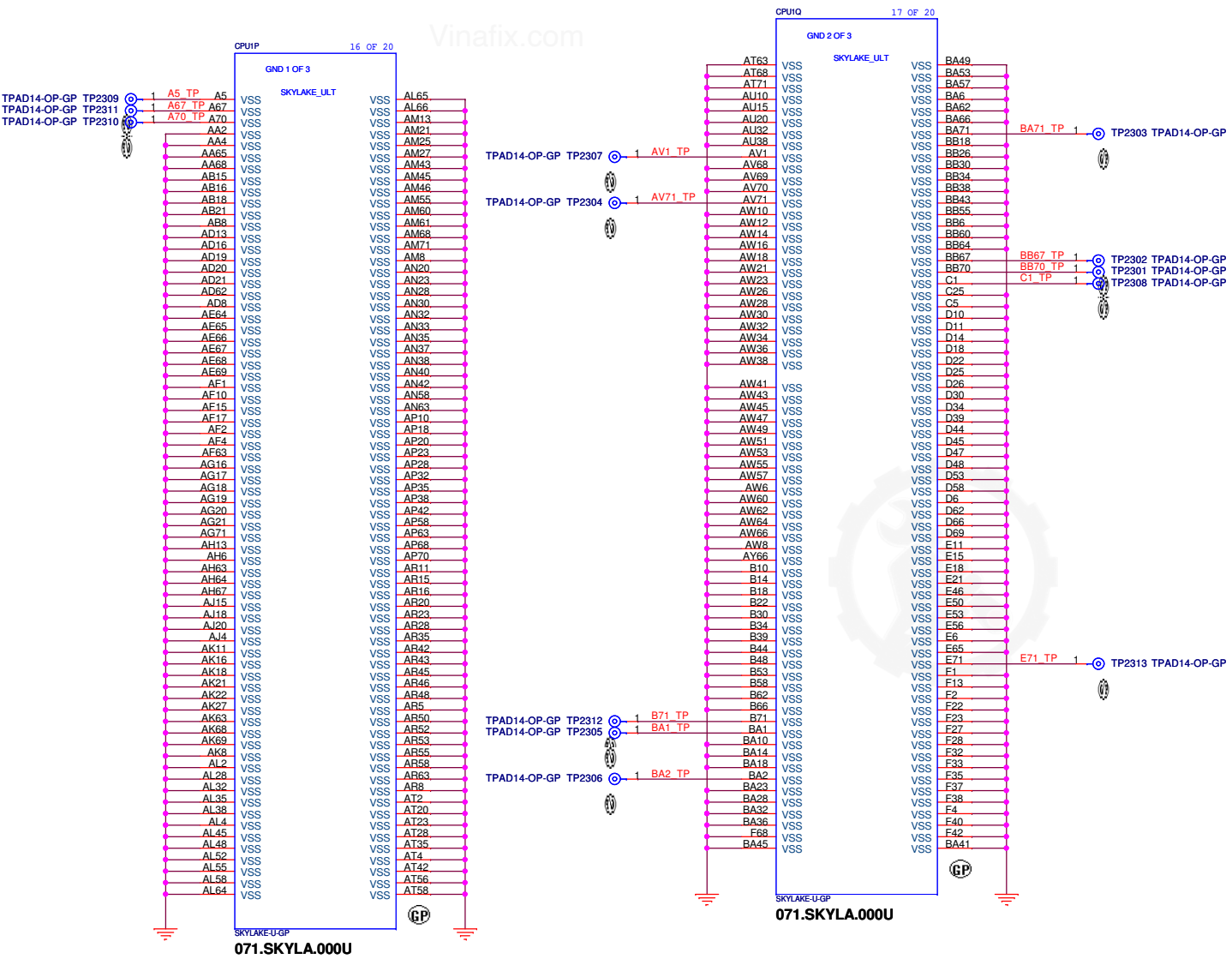
Document Number

Starload SKL-U

Rev
A00

Date: Thursday, February 18, 2016

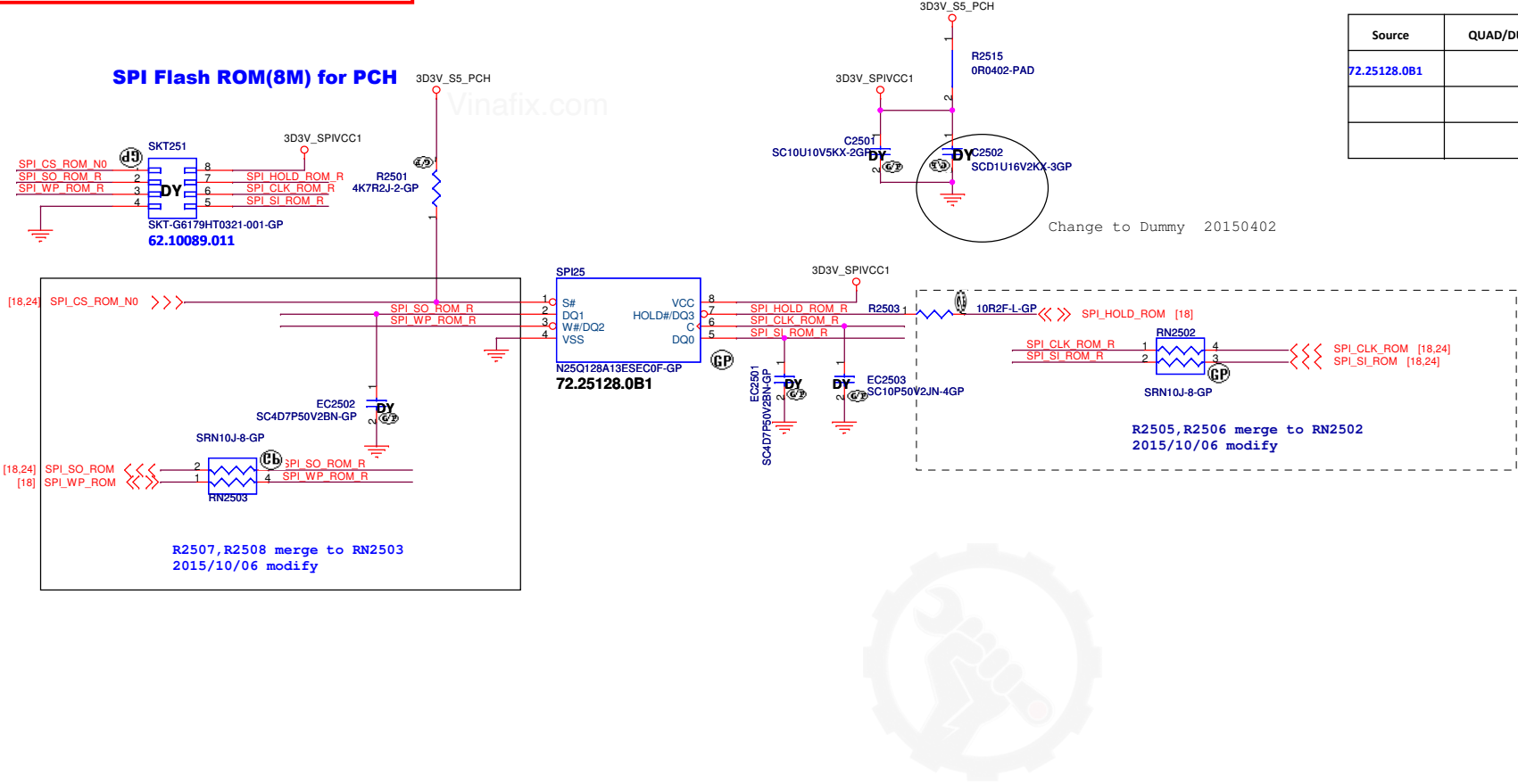
Sheet 22 of 106



Skylake U Processor Corner NCTF Motherboard Test Point Example

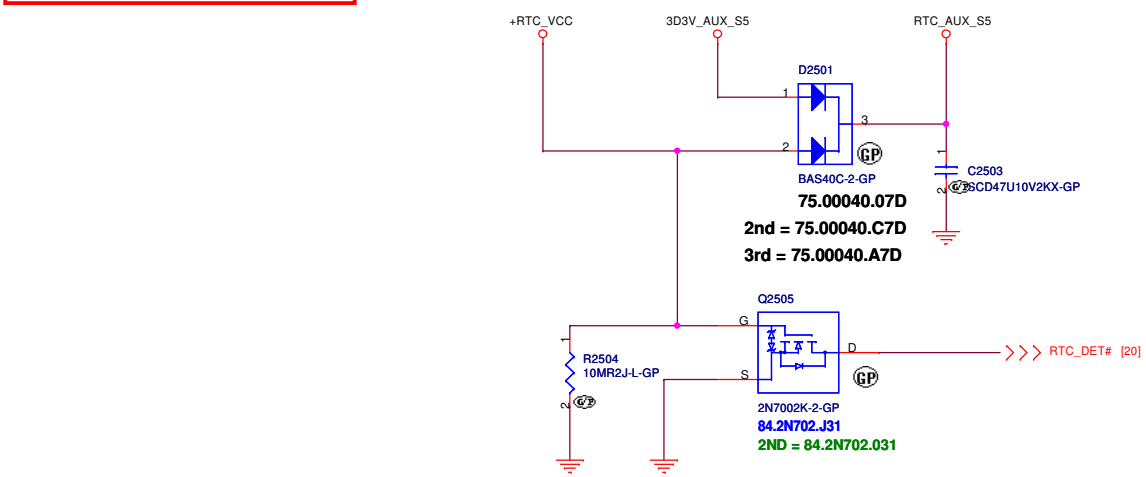
Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	Corner BB1
BA1	NCTFVSS	Test Point (TP)	
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A1
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

Main Func = SPI Flash



Source	QUAD/DUAL fast read	DUAL fast read	SFDP
72.25128.0B1	O	O	O
	O	O	O
	O	O	O

Main Func = RTC



<Core Design>

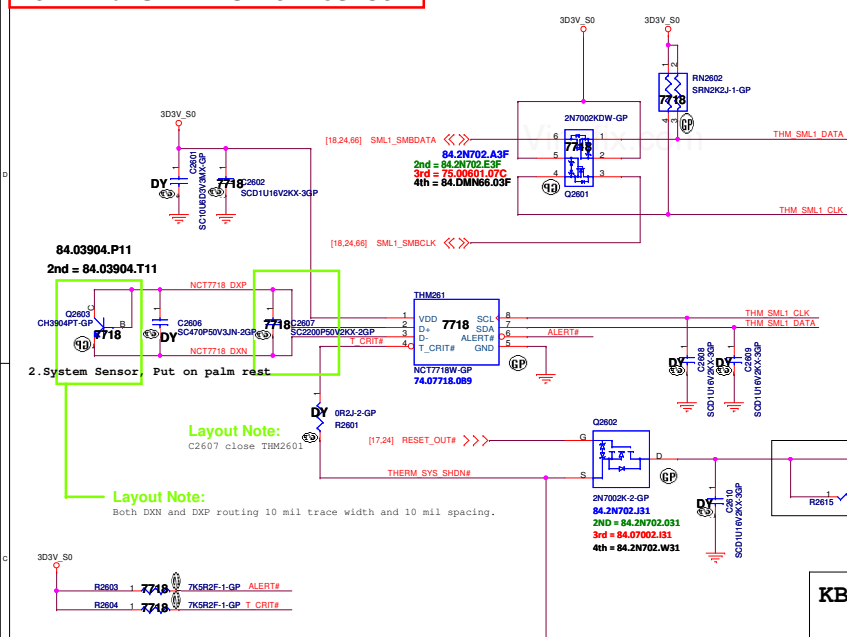
DELL Wistron Corporation

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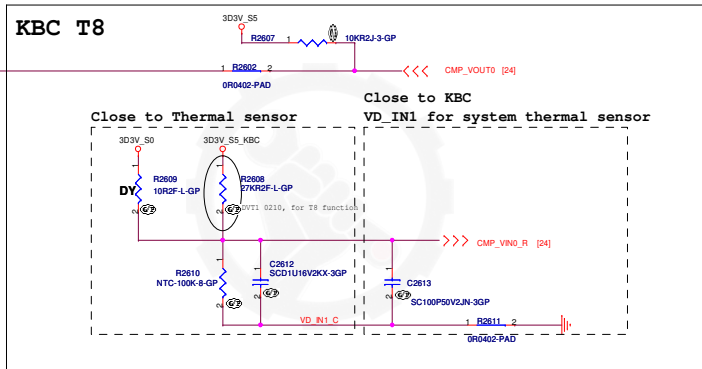
Title **Flash/RTC**

Size A3 Document Number **Starload SKL-U** Rev **A00**

Date: Thursday, February 25, 2016 Sheet 25 of 106

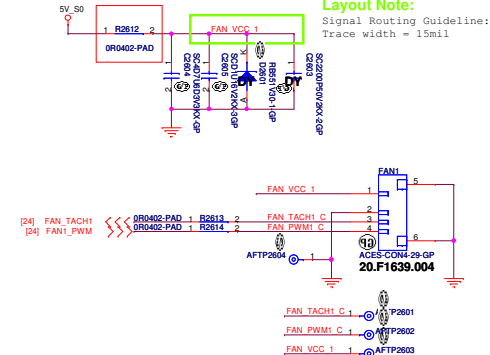


TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



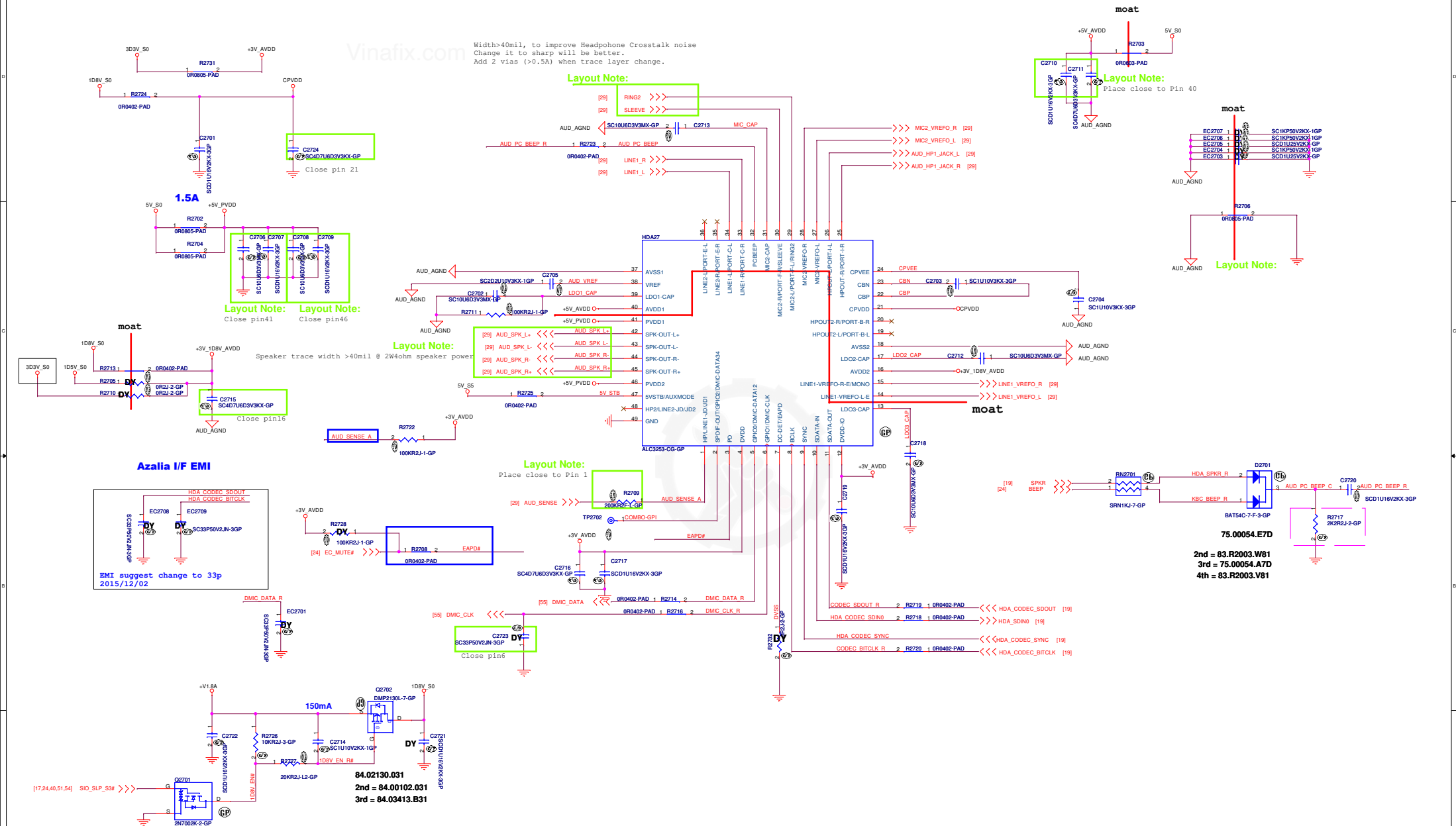
PWM FAN1

Short pad change to 0 ohm , 20141118



<Core Design>

Width>40mil, to improve Headphome Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.



&ltCore Design>



Title			
Audio Codec ALC3246			
Size A2	Document Number		Rev
	Starload SKL-U		A00
Date: Thursday, February 25, 2016		Sheet 27 of	108

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Main Func = Audio

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(Blanking)



<Core Design>



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Title

(Reserved)

Size
A4

Document Number

Starload SKL-U

Rev

A00

Date: Thursday, February 18, 2016

Sheet 30 of 106

Vinafix.com

(Blanking)




Main Func = LAN

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Title

XFOM&RJ45

Size
A3

Document Number
Starload SKL-U

Rev
A00

Date: Thursday, February 18, 2016

Sheet 32 of 106

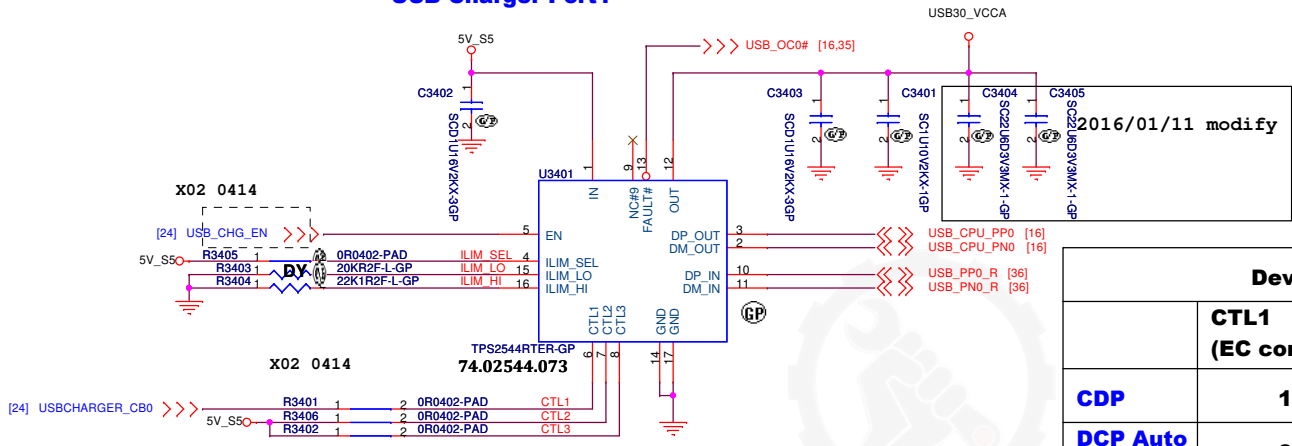
Vinafix.com

(Blanking)



Vinafix.com

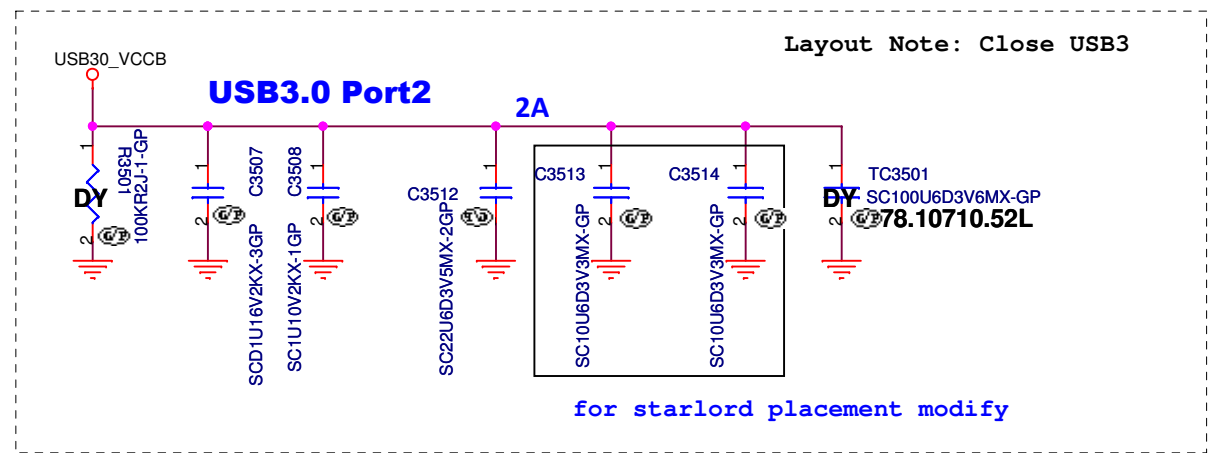
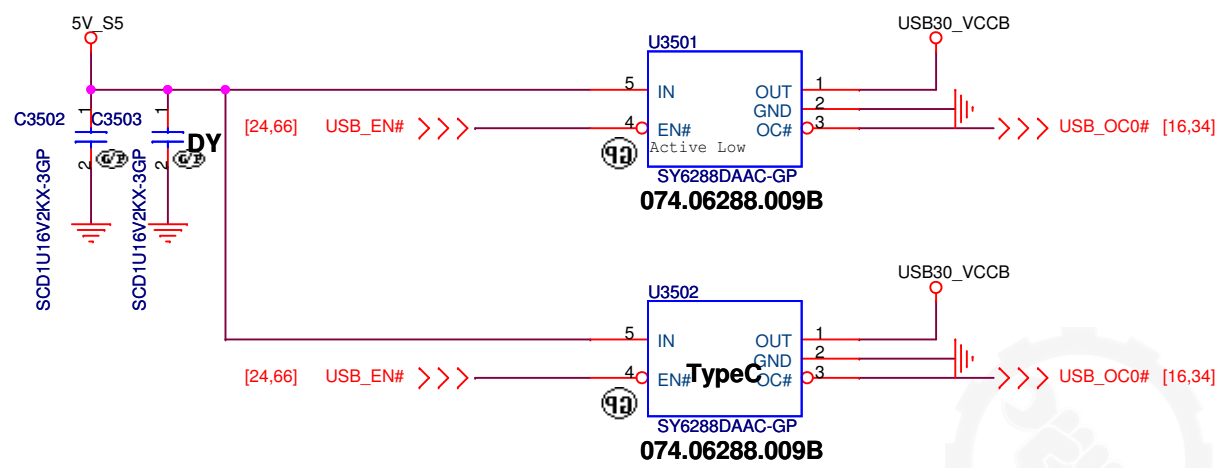
USB Charger Port1




Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

Main Func = USB3.0 Port1

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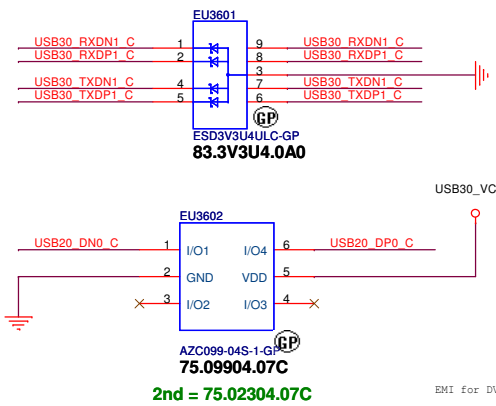
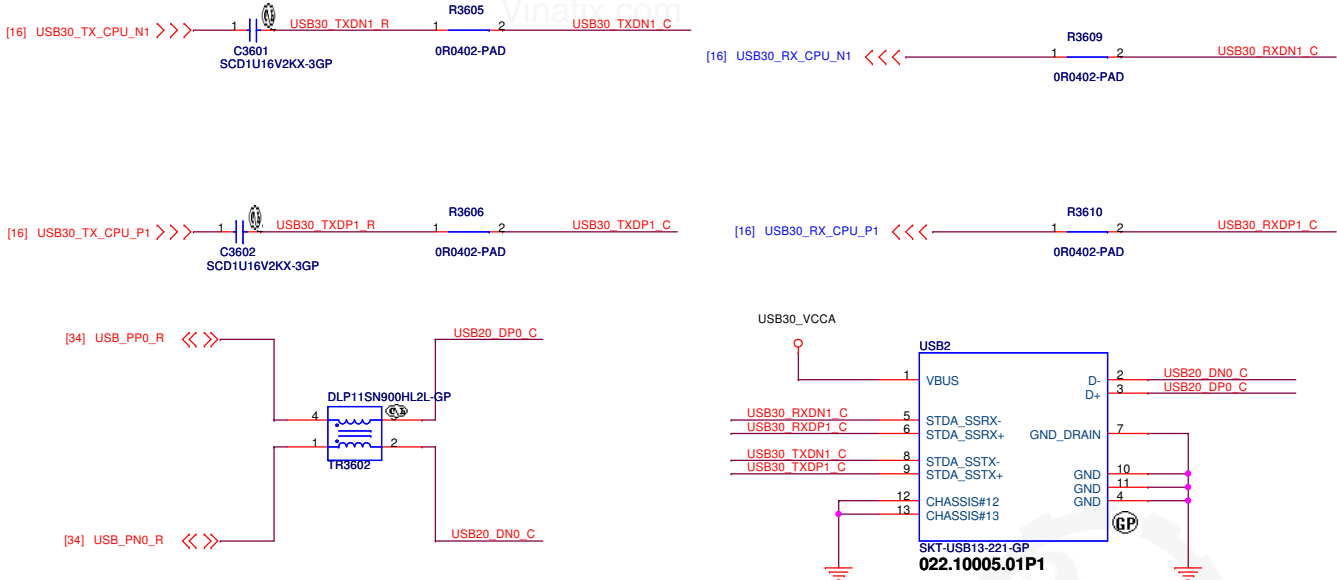
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Title USB switch			
Size	Document Number Starload SKL-U		Rev A00
Date: Thursday, February 25, 2016		Sheet 35 of	106

Main Func = USB3.0 Port1

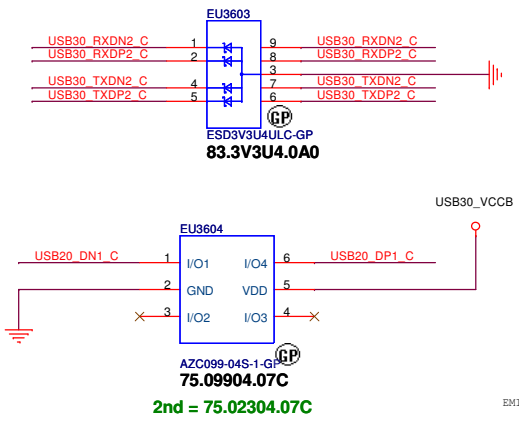
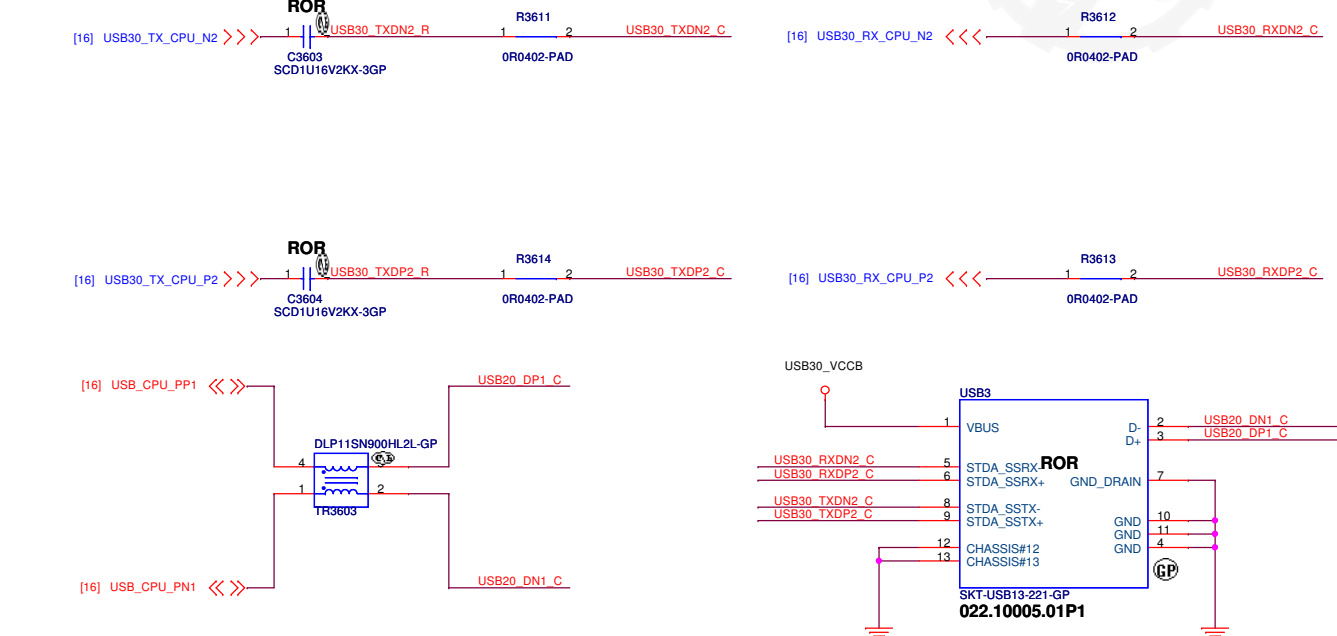
USB2.0 Port2 and USB2.0 Port3 are on IOBD

USB3.0 Port1



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

USB3.0 Port2



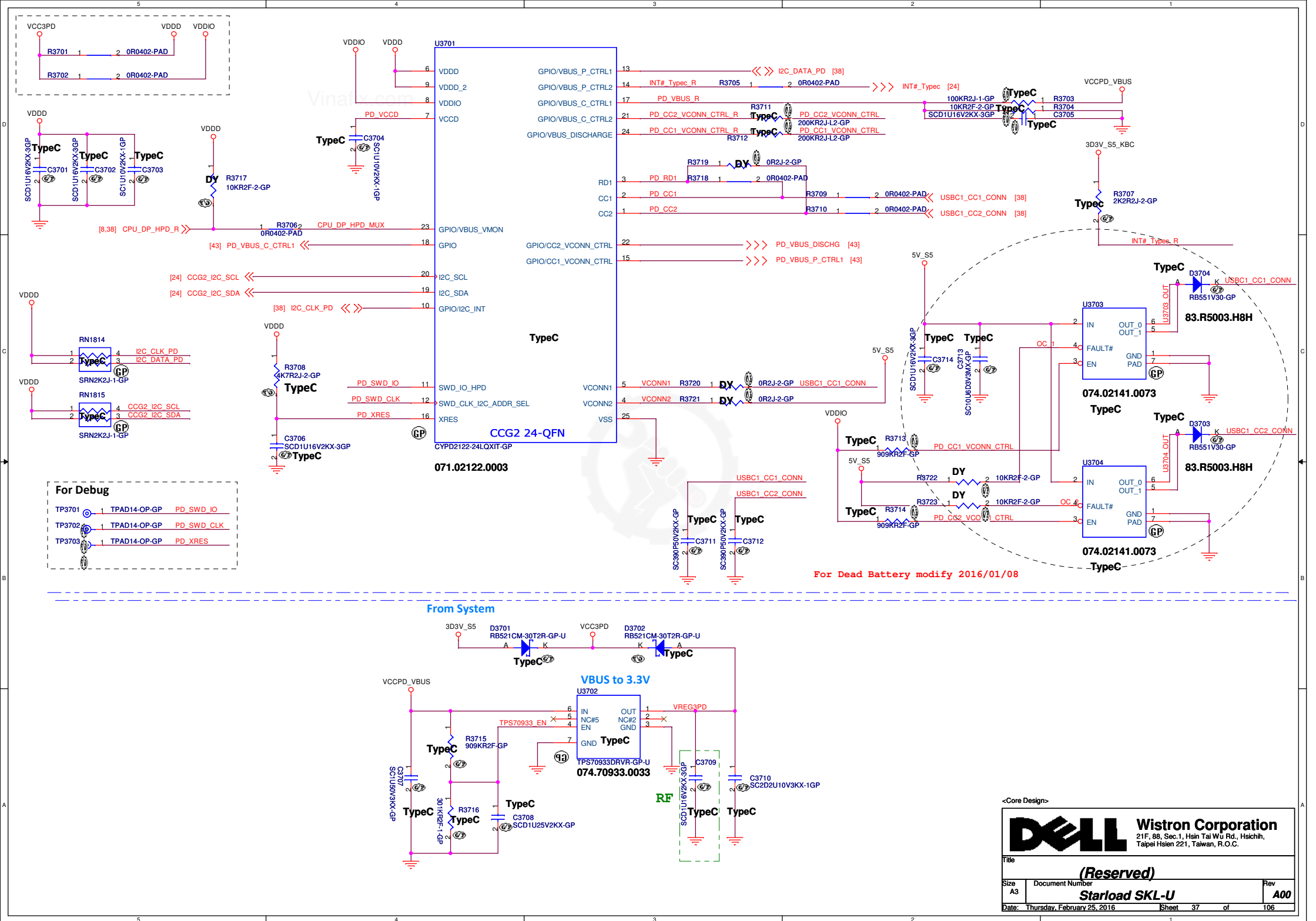
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Taipei Hsien 221, Taiwan, R.O.C.

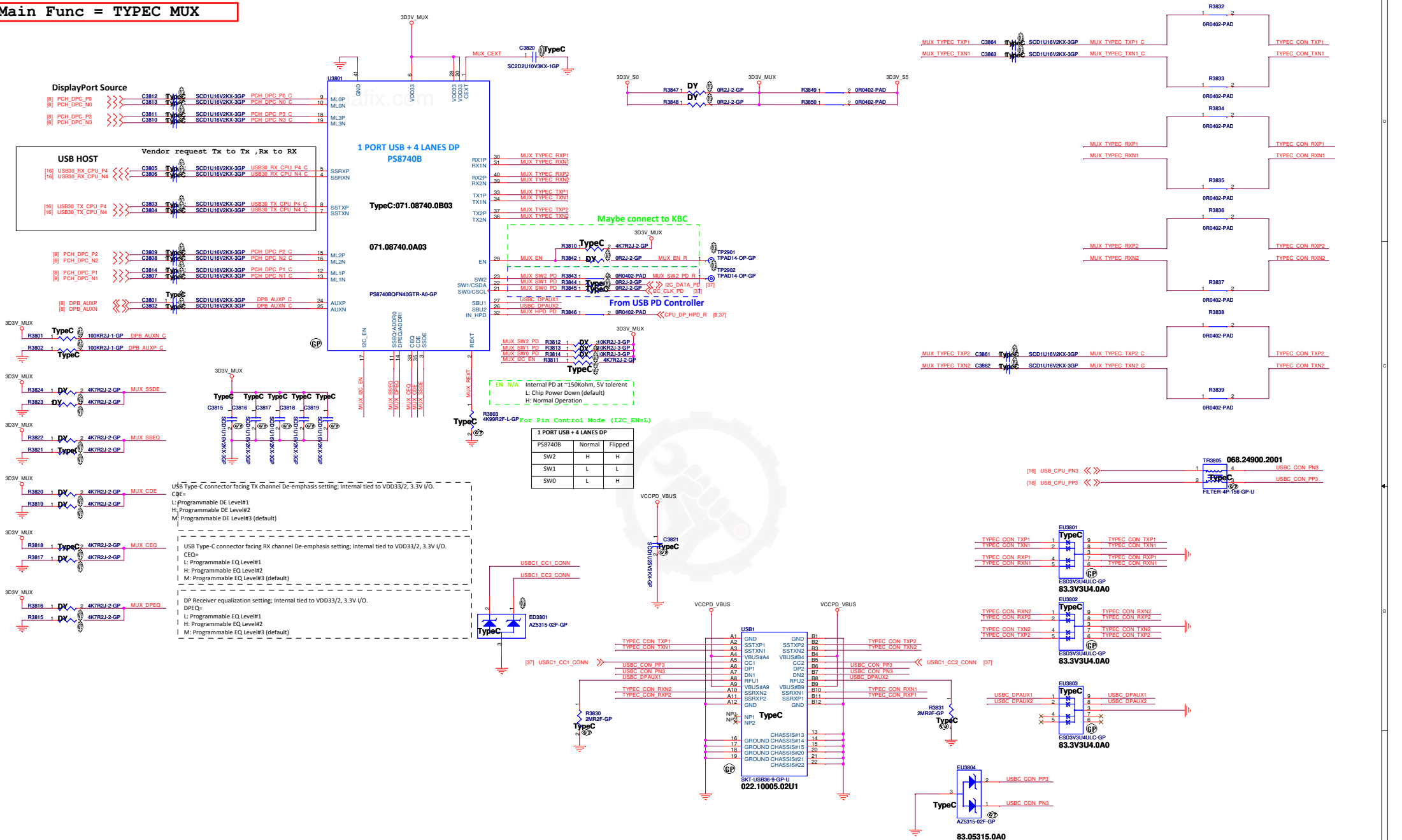
Title: **USB30**

Size A3 Document Number: **Starload SKL-U** Rev: **A00**

Date: Thursday, February 25, 2016 Sheet 36 of 106

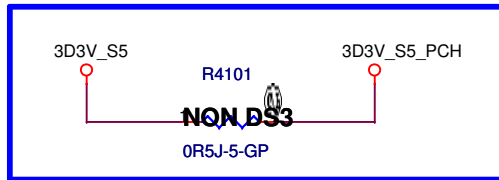


Main Func = TYPEC MUX

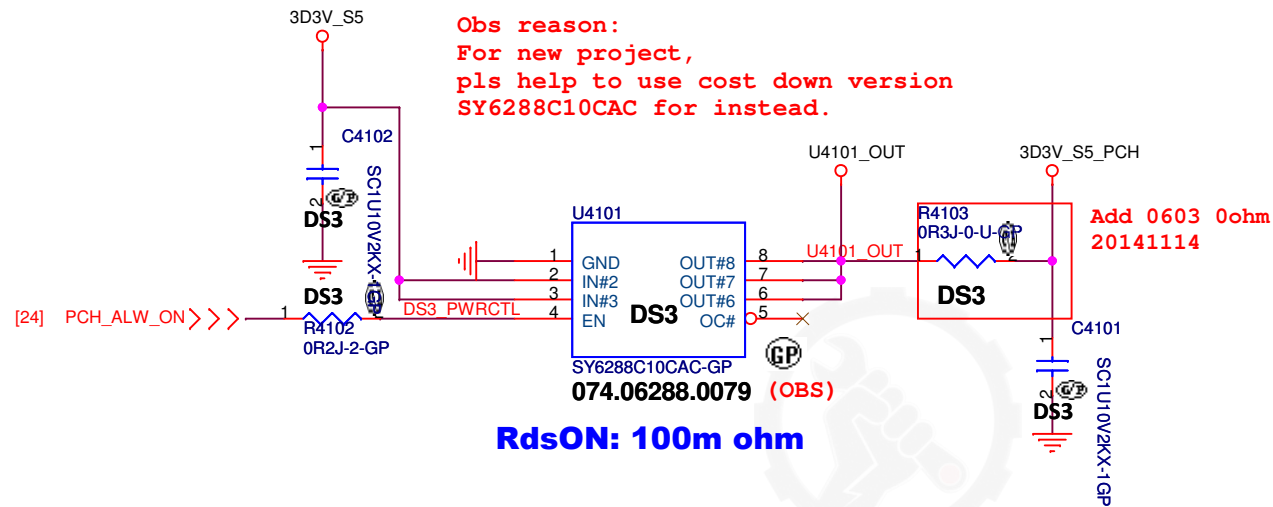


Main Func = Power Plane & Sequence

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Reserve by NON DS3 function 20150413



DS3

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Title

Connected_Standby(1/2)+DS3

Size
A4

Document Number

Starload SKL-U

Rev
A00

Date: Thursday, February 25, 2016


Sheet 41 of 106

Main Func = DIMM1
Main Func = DIMM2

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Title

Connected_Standby(2/2)

Size

A3

Date: Thursday, February 18, 2016

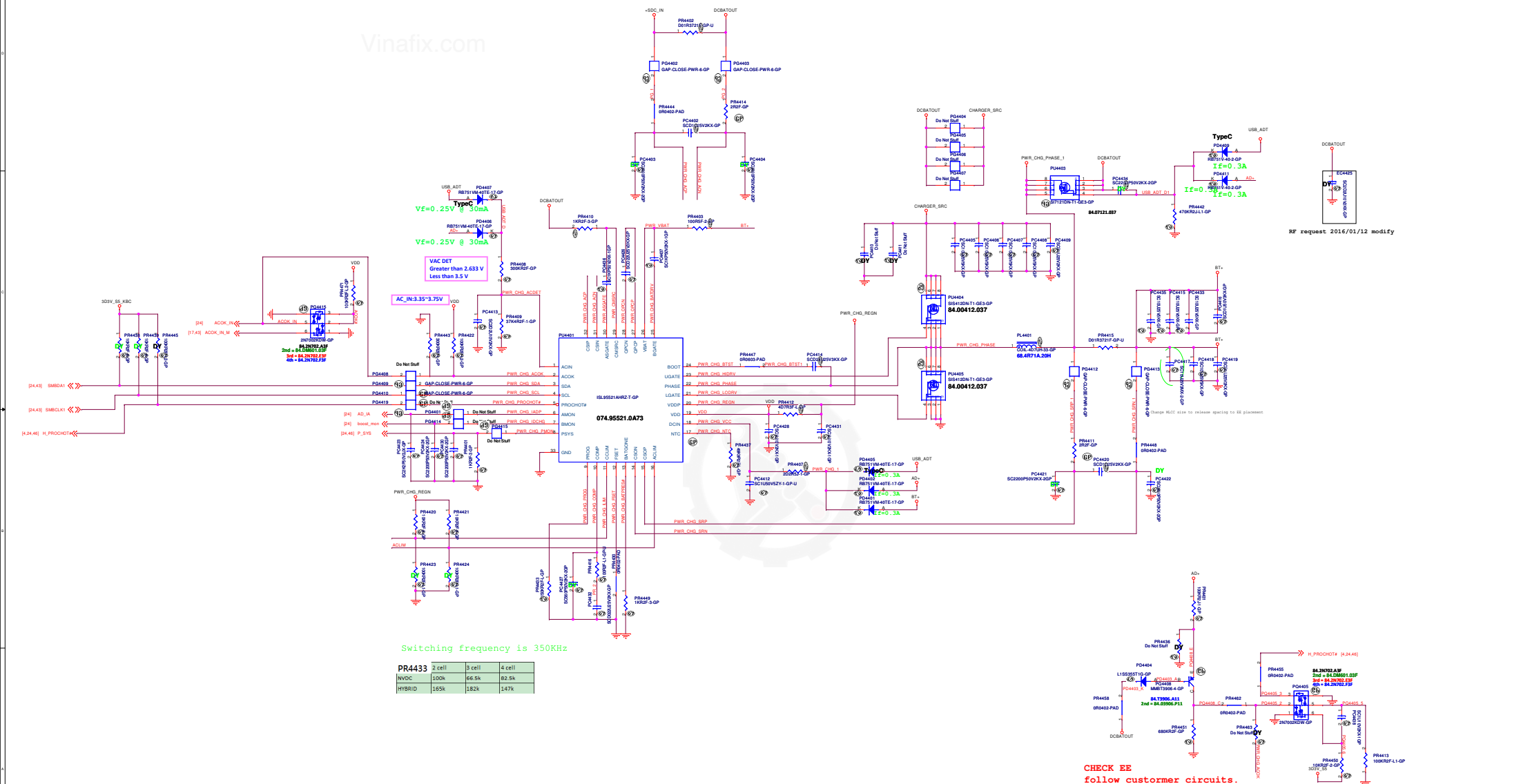
Document Number

Starload SKL-U

Sheet 42 of 106

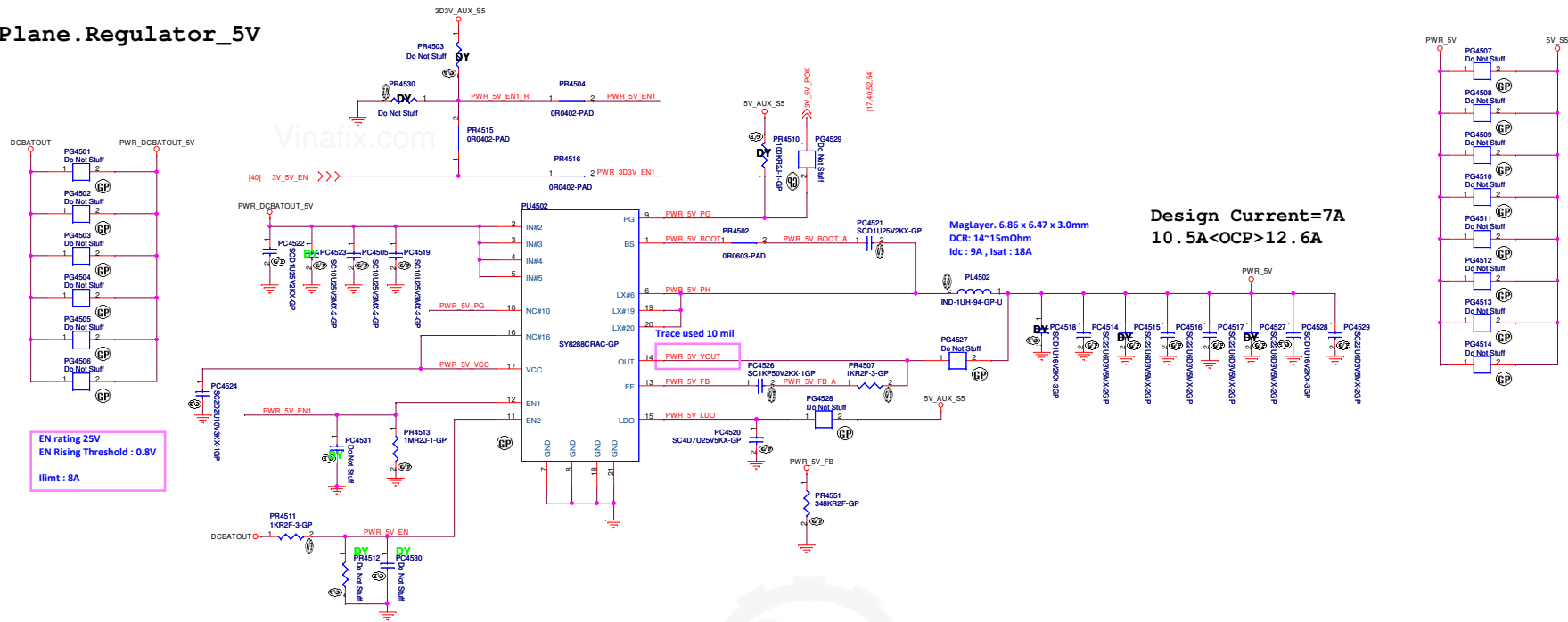
Rev

A00

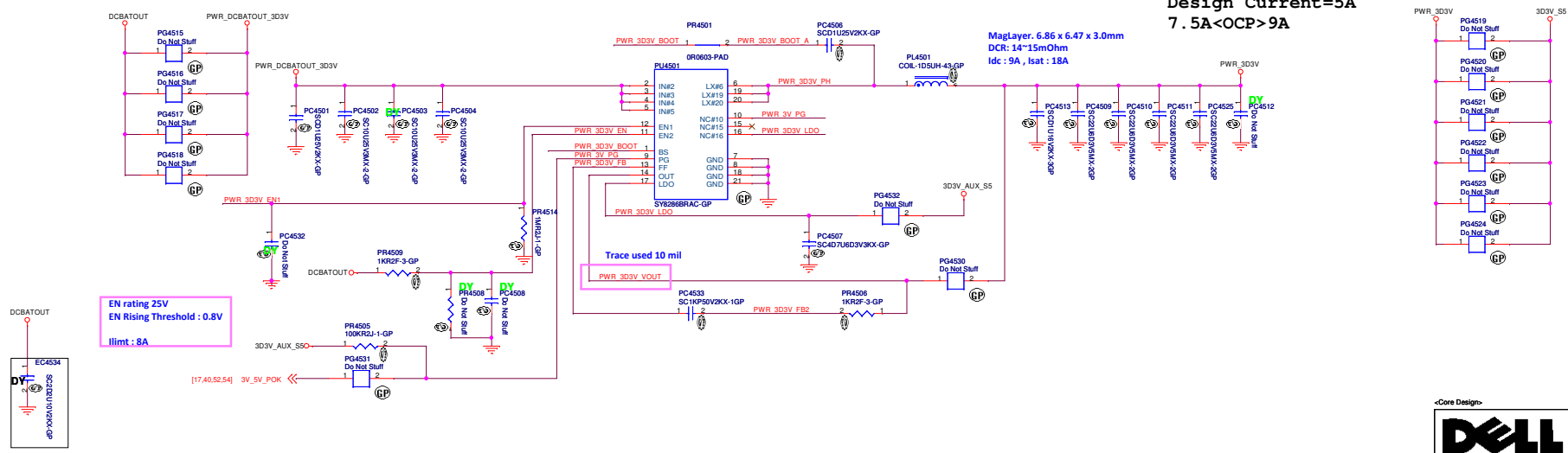


CHECK EE
follow customer circuits.

SSID = PWR.Plane.Regulator_5V

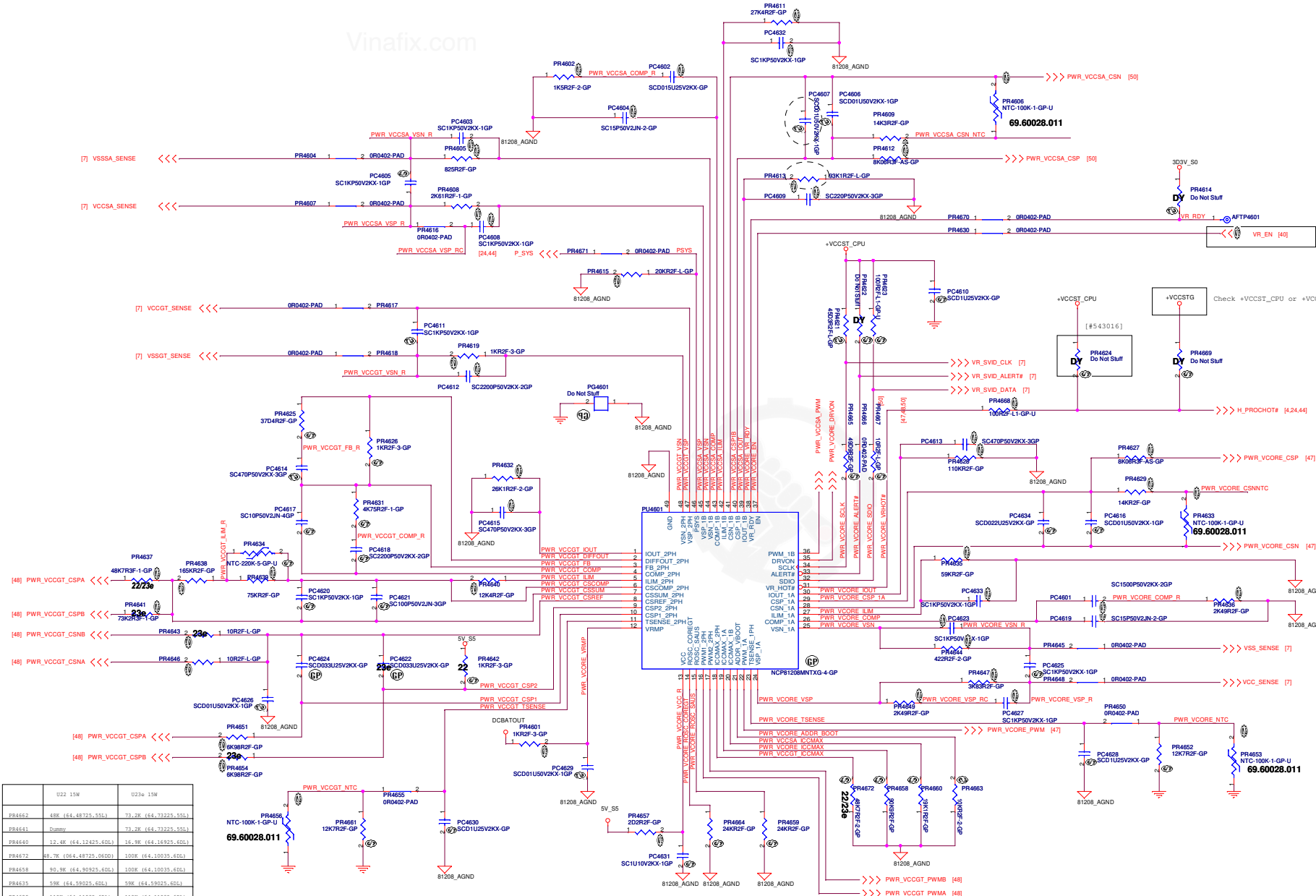


SSID = PWR.Plane.Regulator_3D3V



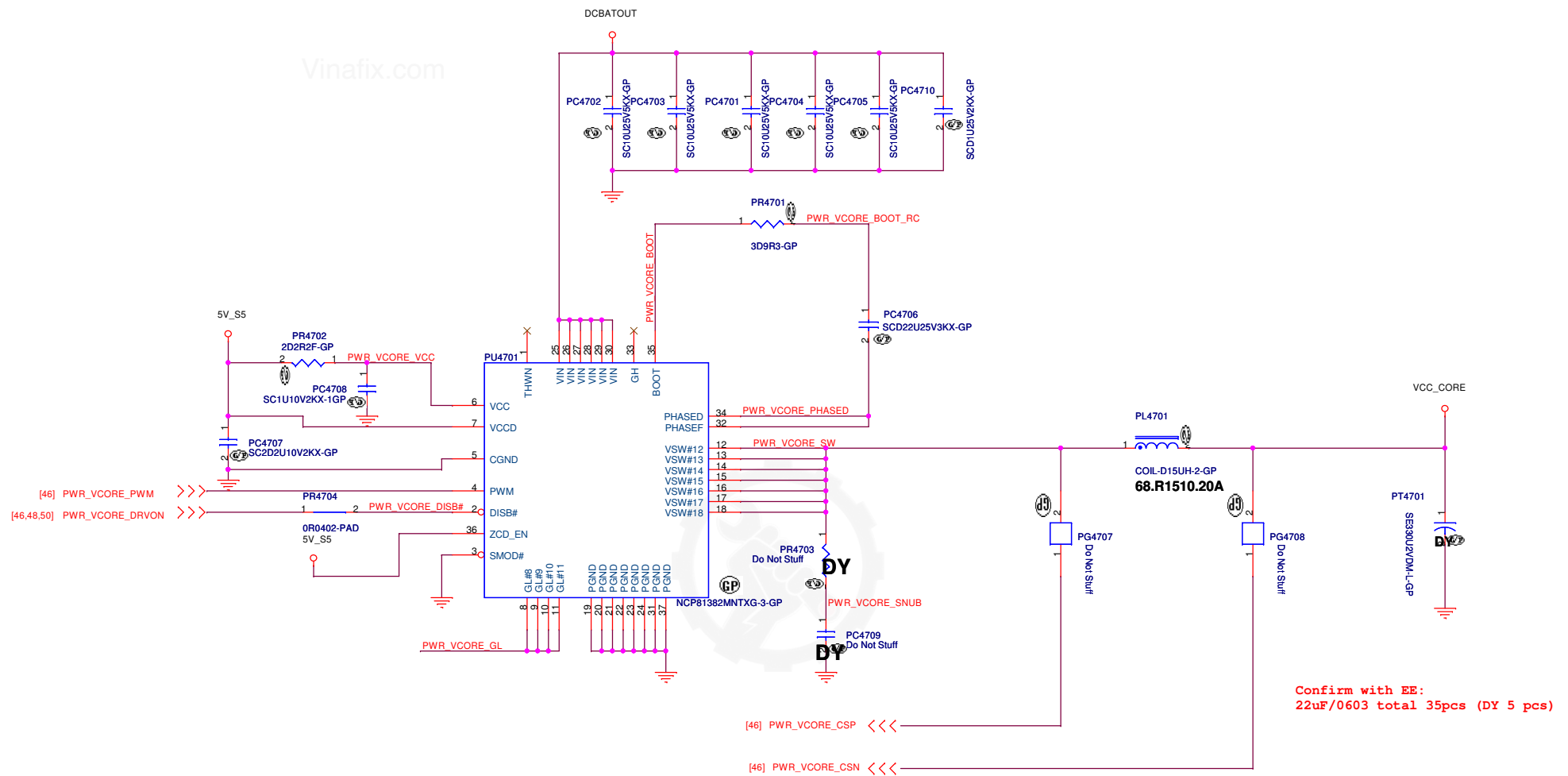
Main Func = CPU_CORE

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	U22 15W	U23a 15W
PR4662	48K (64,48725,55L)	72.2K (64,73225,55L)
PR4641	Dummy	72.2K (64,73225,55L)
PR4640	12.4K (64,12425,60L)	16.9K (64,16925,60L)
PR4672	48.7K (64,48725,60D)	100K (64,10035,60L)
PR4658	90.9K (64,90925,60L)	100K (64,10035,60L)
PR4635	59K (64,59025,60L)	59K (64,59025,60L)
PR4628	110K (64,11035,60L)	110K (64,11035,60L)
PR4643	Dummy	10K (64,10805,60L)
PR4654	Dummy	6.98K (64,69815,60L)
PC4624	Dummy	0330 (78,33222,2FL)
PR4642	1K (64,10035,60L)	Dummy
PR4602	1.5K (64,15035,60L)	1.5K (64,15035,60L)
PC4602	15n (78,15322,2FL)	15n (78,15322,2FL)

Main Func = CPU_CORE



<Core Design>



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Title

NCP81382MN_CPU_VCORE(2/3)

Size
A3

Document Number

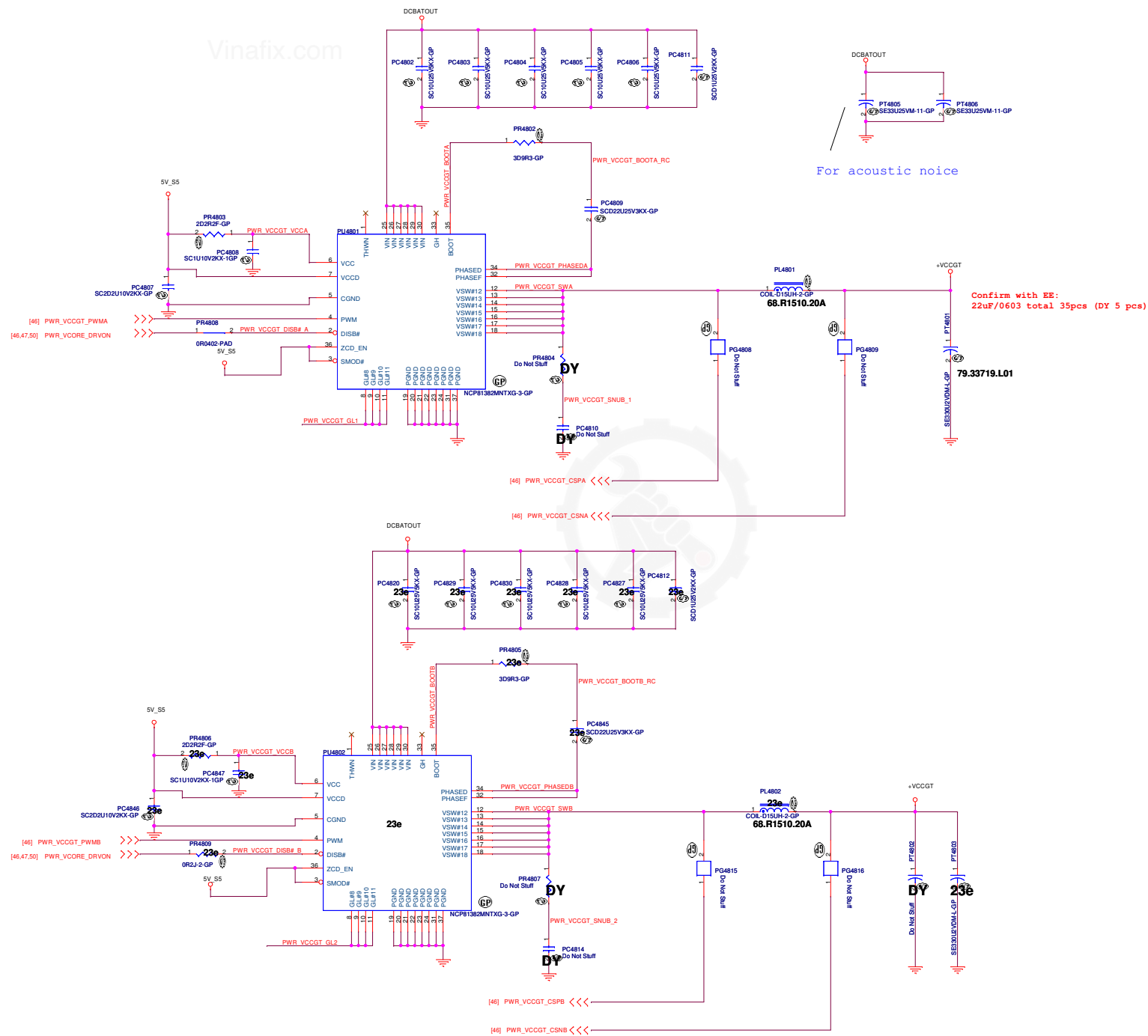
ment Number
Starload SKL-U

A00

Date: Thursday, February 25, 2016

Sheet 47 of 106

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Main Func = CPU_CORE
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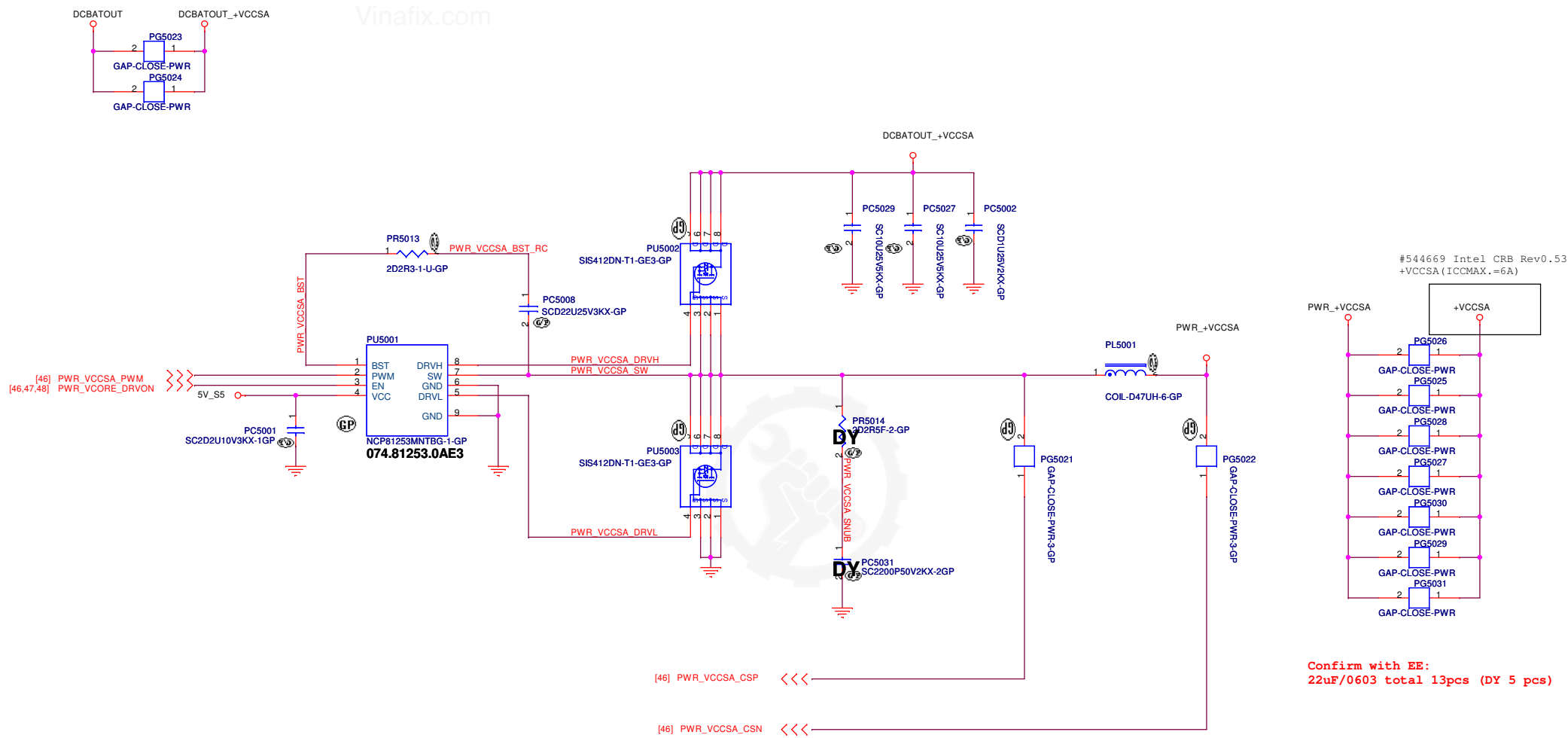
<Core Design>

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Title **NCP81382MN_CPU_VCCGT(3/3)**

Size A2	Document Number Starload SKL-U	Rev A00
Date: Thursday, February 25, 2016		Sheet 48 of 106

Main Func = CPU_CORE

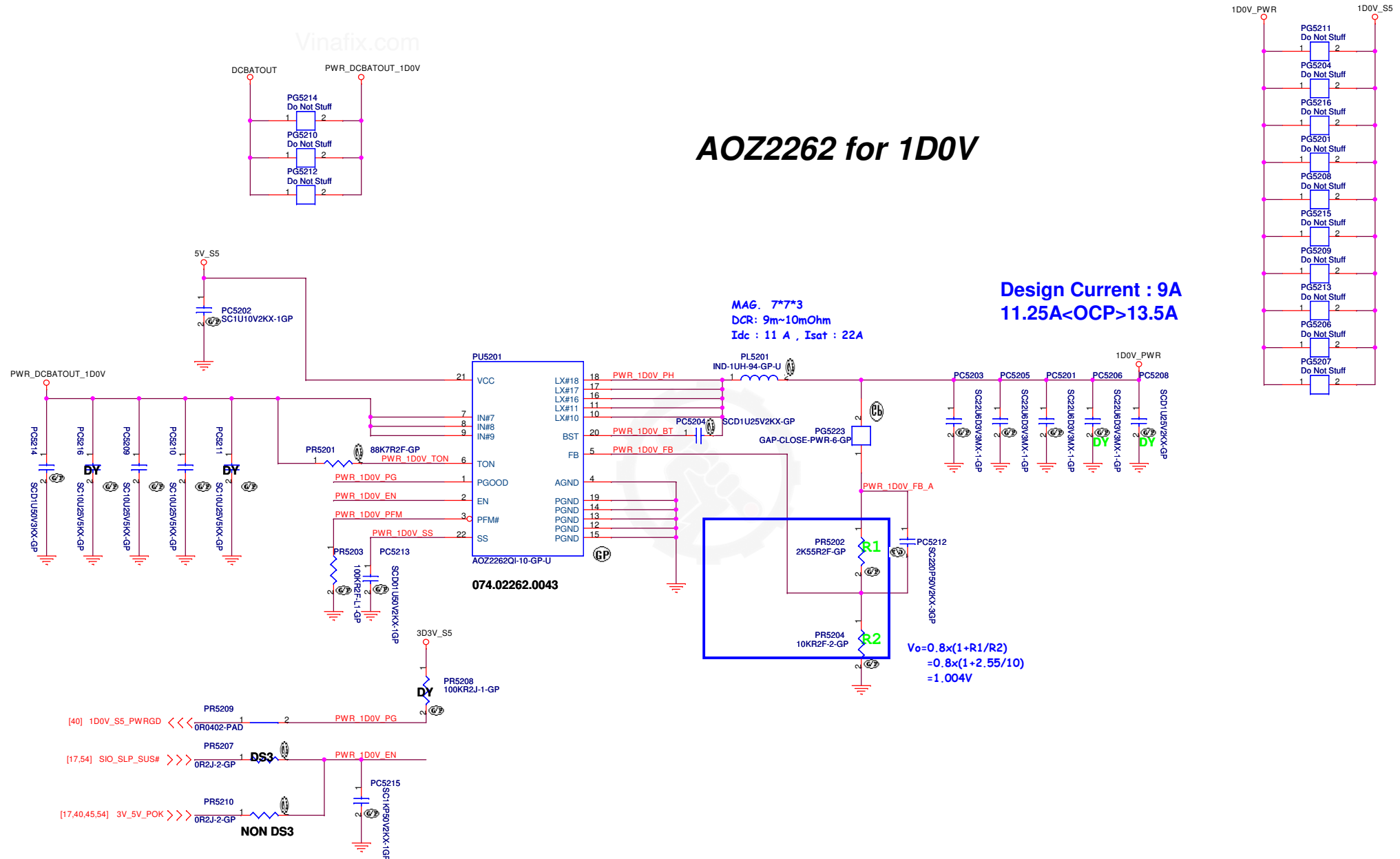


SSID = PWR.Plane.Regulator_1D0V

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AOZ2262 for 1D0V

Design Current : 9A
11.25A<OCP>13.5A



<Core Design>

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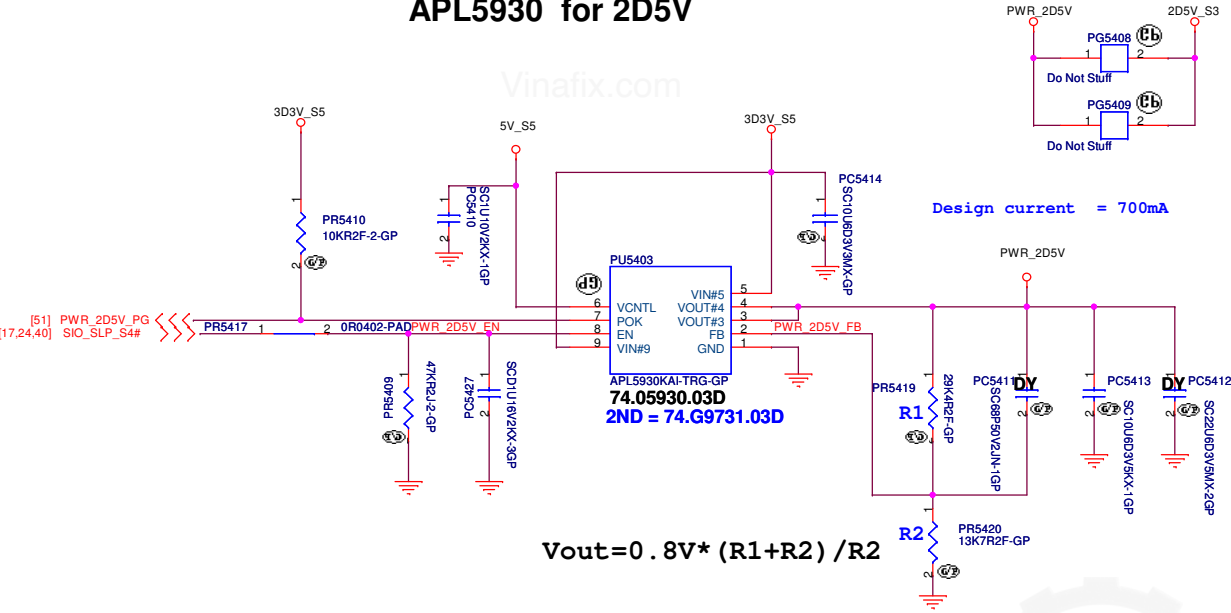


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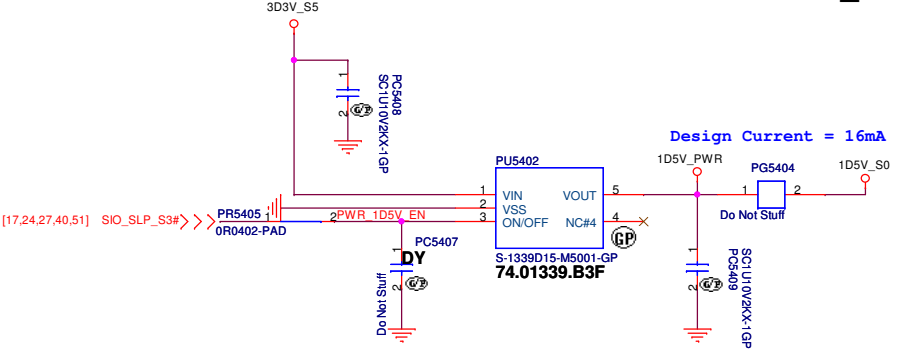
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserved)			
Size	Document Number		Rev
A3	Starload SKL-U		A00
Date: Thursday, February 18, 2016		Sheet 53 of	106

Main Func = 1D5V

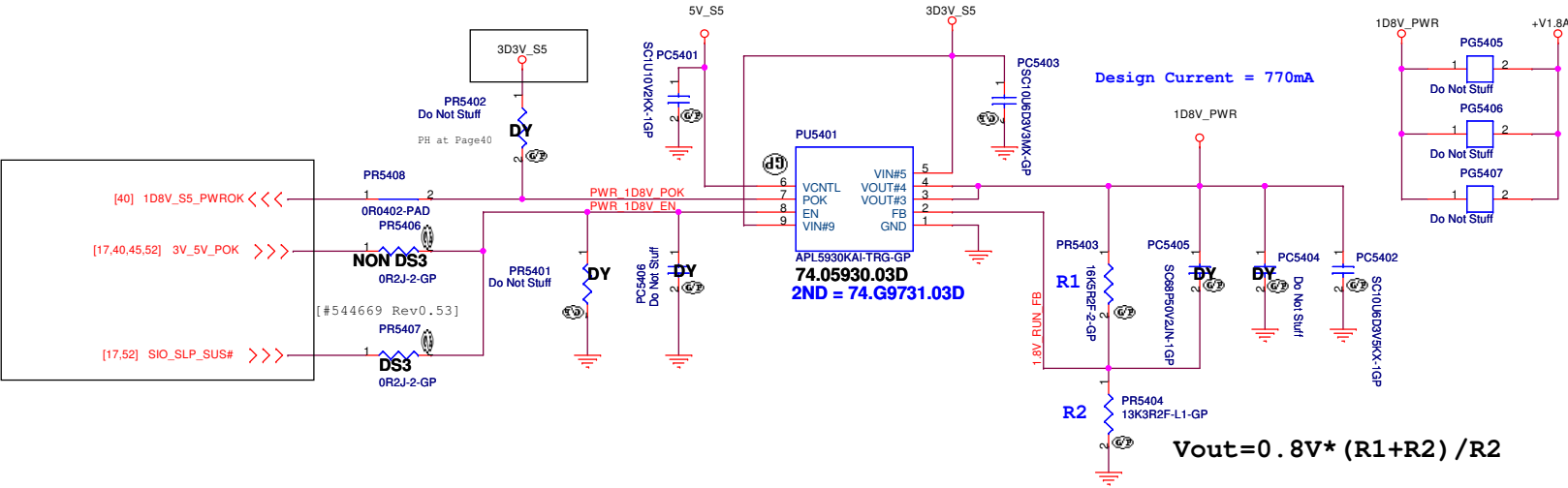
APL5930 for 2D5V

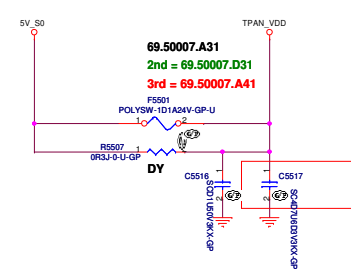
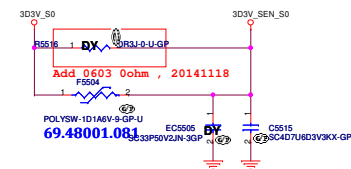
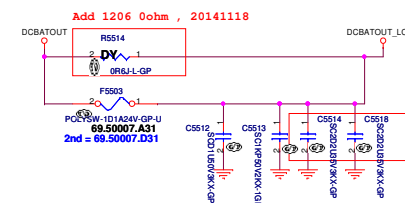
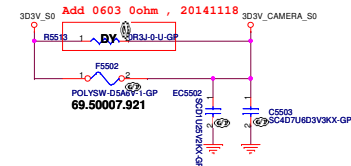
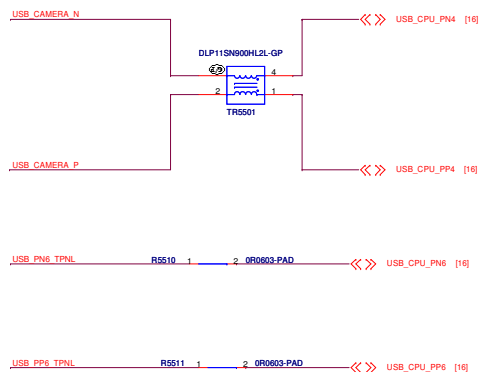
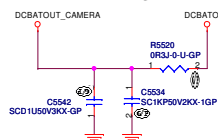
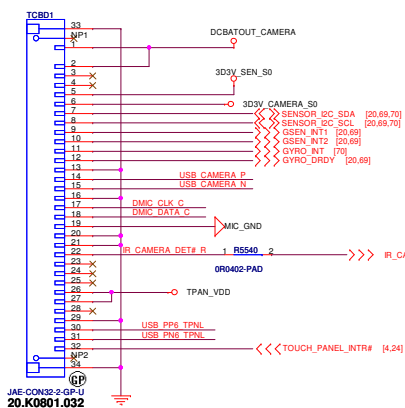
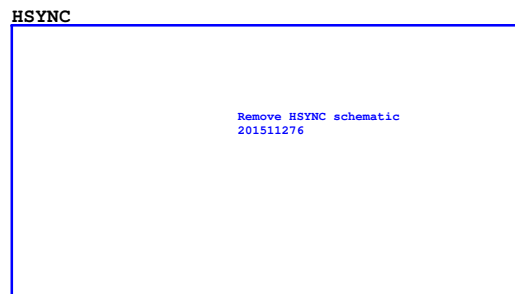


S-1339D15-M5001 for 1D5V_S0



APL5930 for 1D8V_S5



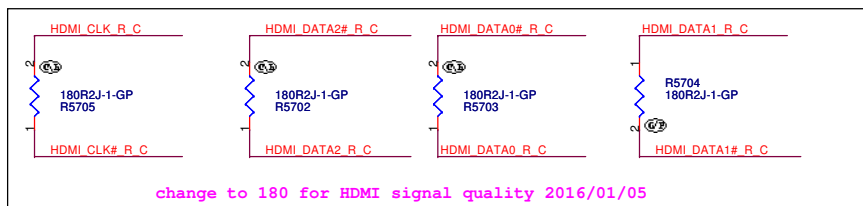
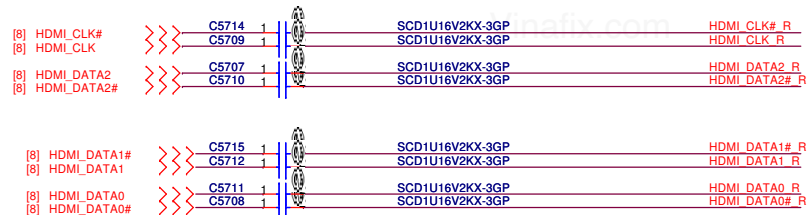


		Wistron Corporation 21F, 68, Sec.1, Hsin Tai Wu Rd., Hsueh, Taipei Hsien 221, Taiwan, R.O.C.	
Title CRT			
Size A2	Document Number Starload SKL-U		Rev A00
Date: Thursday, February 18, 2016		Sheet 56 of 106	

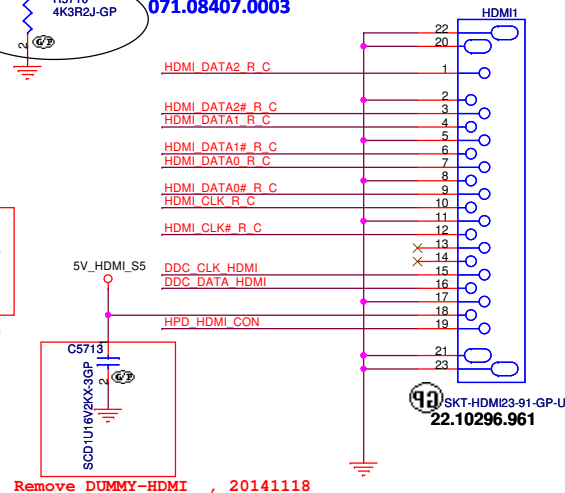
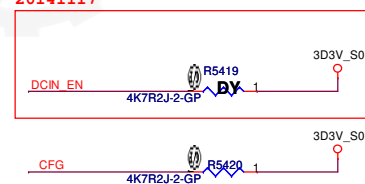
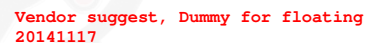
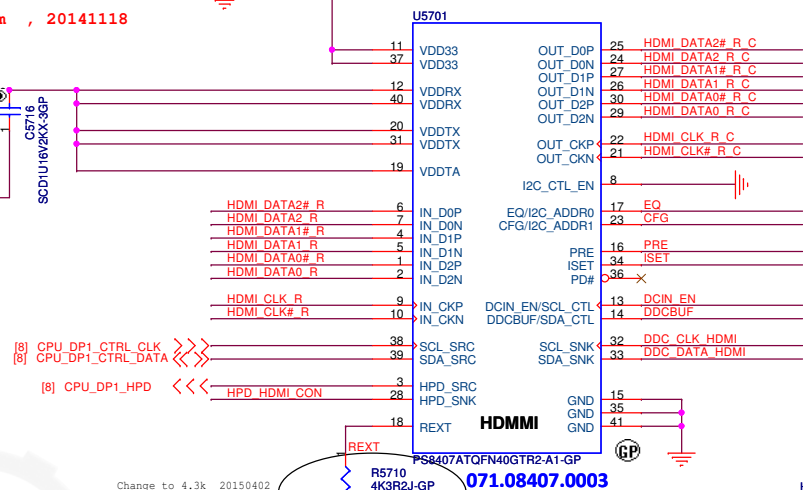
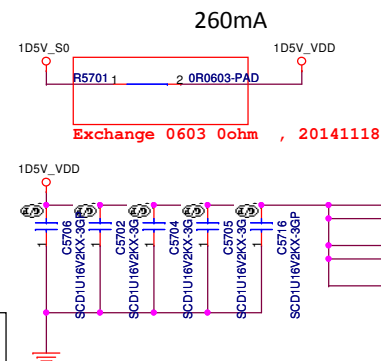
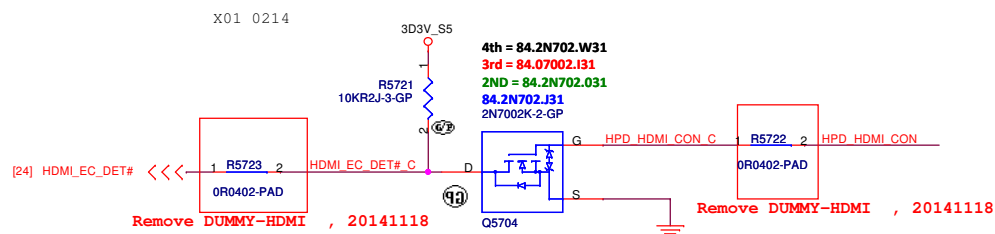
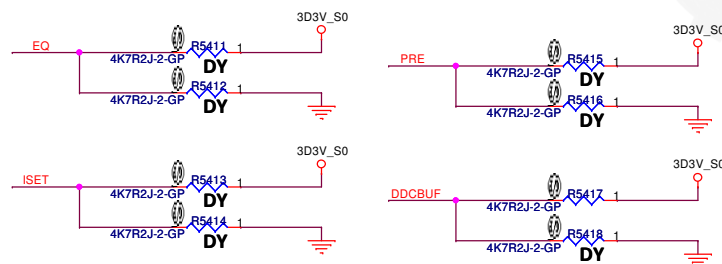
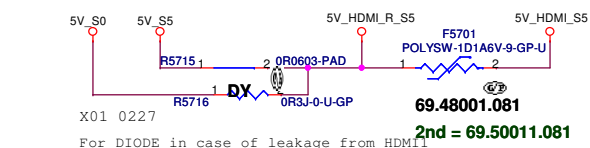
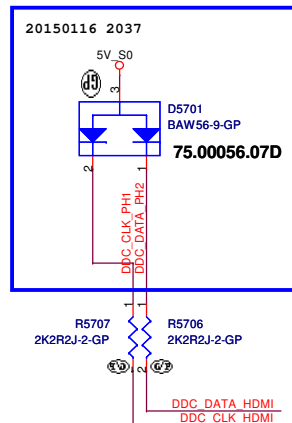
Wistron Corporation
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Title			
CRT			
Size A2	Document Number		Rev
	Starload SKL-U		A00
Date:	Thursday, February 19, 2016	Sheet	56 of 106

Main Func = HDMI



Change symbol part number, because origin symbol is DELL OBS part



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Title

(Reserved)

Size

A3

Document Number

Starload SKL-U

Rev

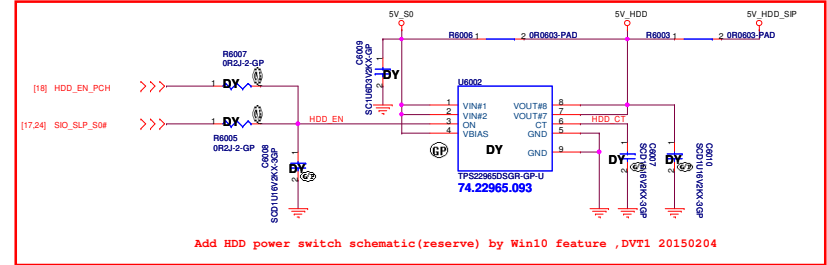
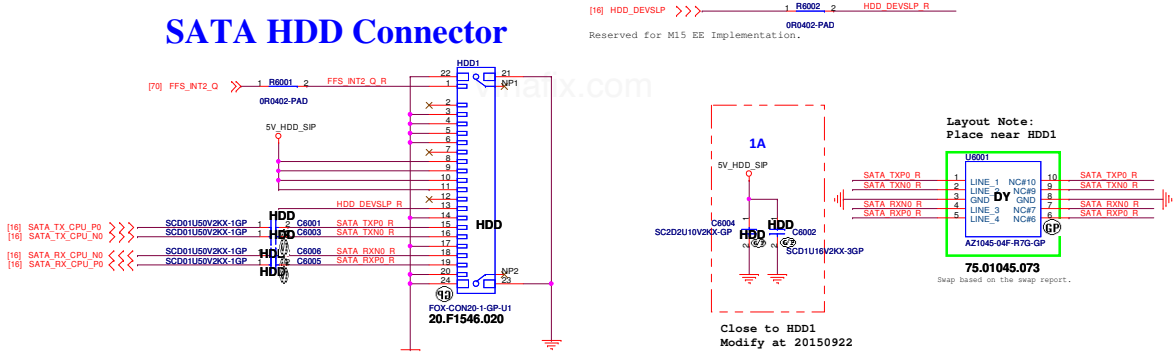
A00

Date: Thursday, February 18, 2016

Sheet 59 of 106

Main Func = HDD

SATA HDD Connector




Main Func = ODD

Main Func = WLAN

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Title

NGFF WLAN CONN


Size	Document Number	Rev
A3	Starload SKL-U	A00

Date: Thursday, February 18, 2016	Sheet 61 of 106
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<Core Design>

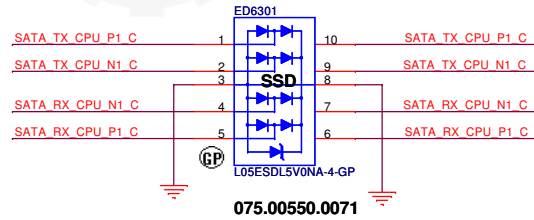
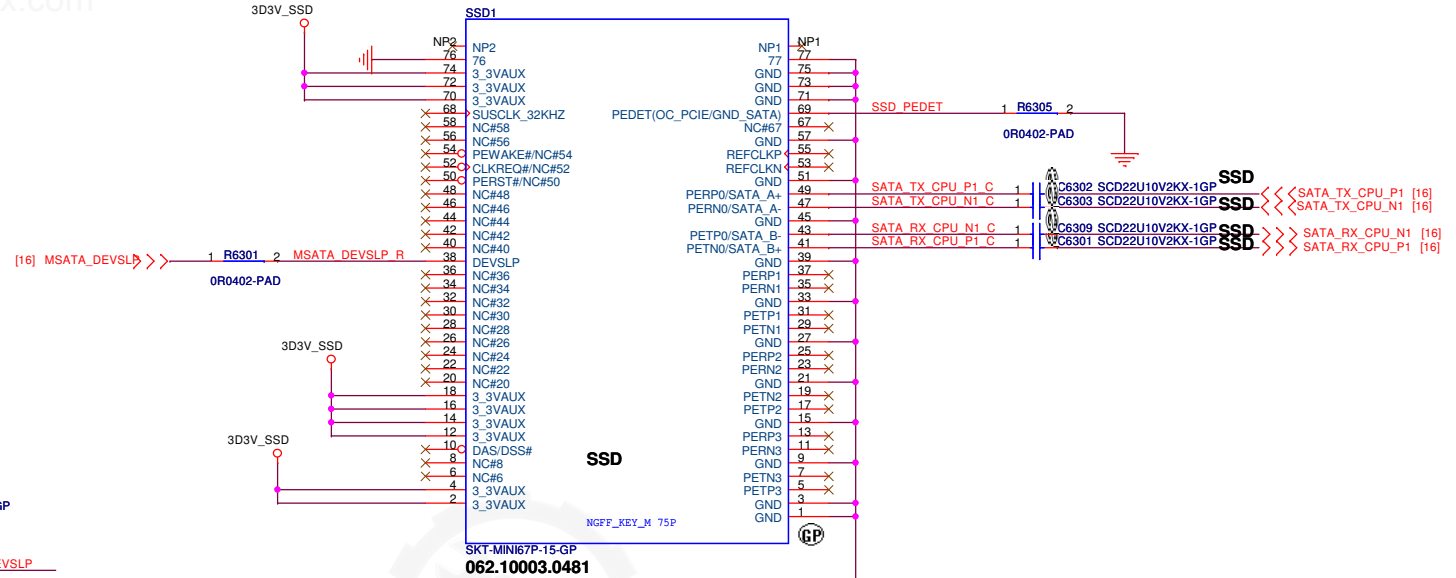
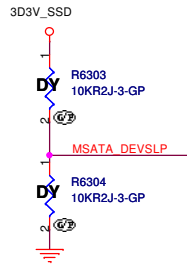
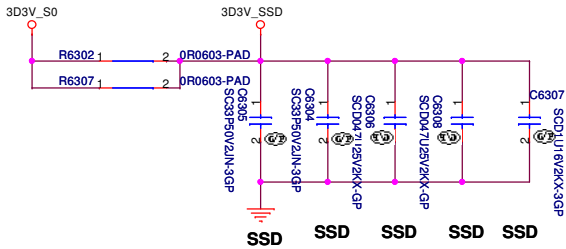
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Title			
Reserved			
Size A4	Document Number Starload SKL-U		Rev A00
Date: Thursday, February 18, 2016		Sheet 62 of	106

SSD M.2

- Important!** SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.
- This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
 - When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

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SSD M.2 CONN



<Core Design>



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Title			(Reserved)	
Size	Document Number	Starload SKL-U		Rev
A3				A00
Date: Thursday, February 25, 2016		Sheet	63	of 106

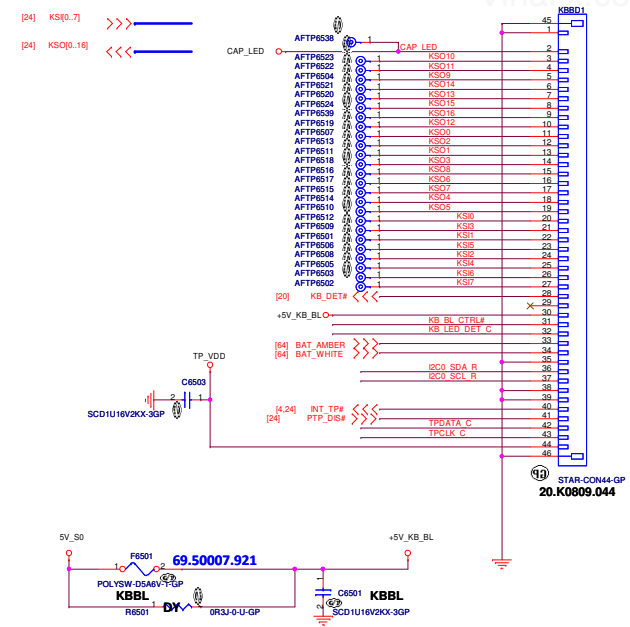
Low activated from KBC GPIO



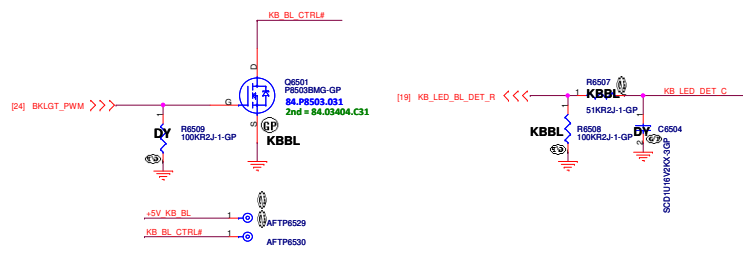
Low activated from KBC GPIO



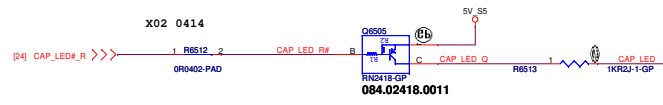
Keyboard



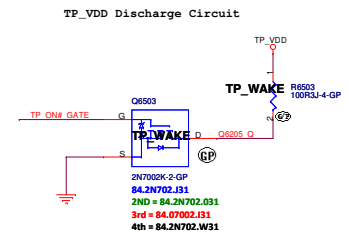
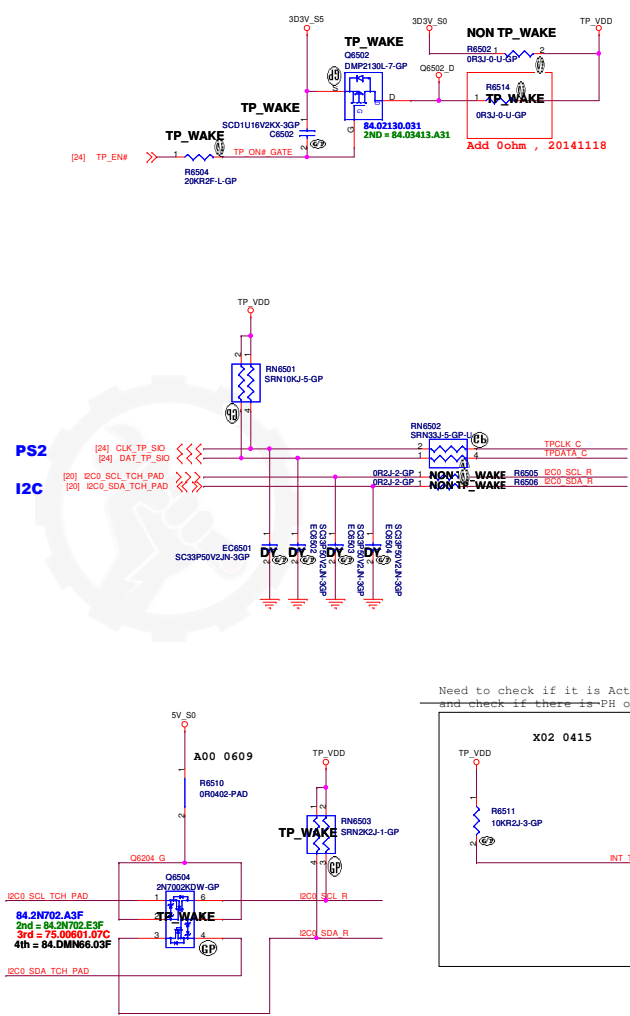
KB Backlight Power Consumption: 285mA max.



CAP LED Control
LOW actived from KBC GPIO



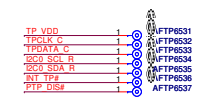
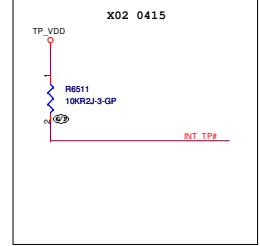
3
Main Func = TPAD



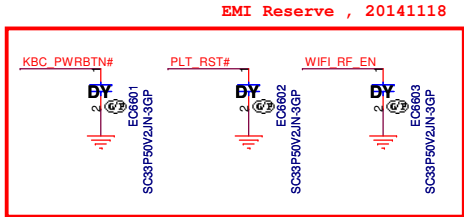
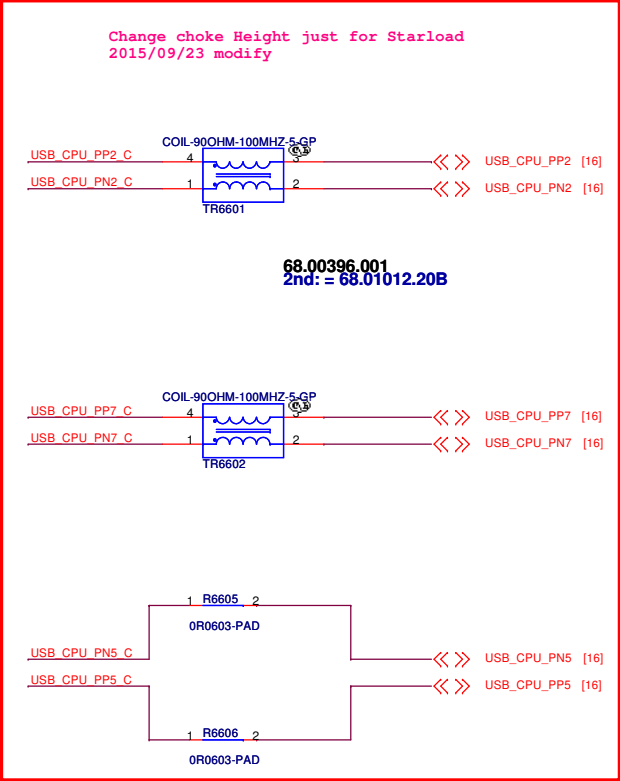
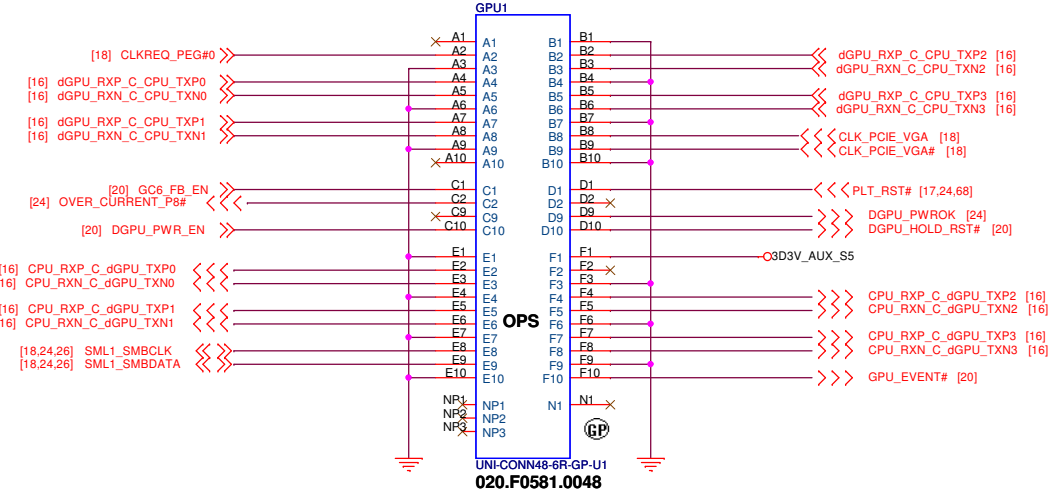
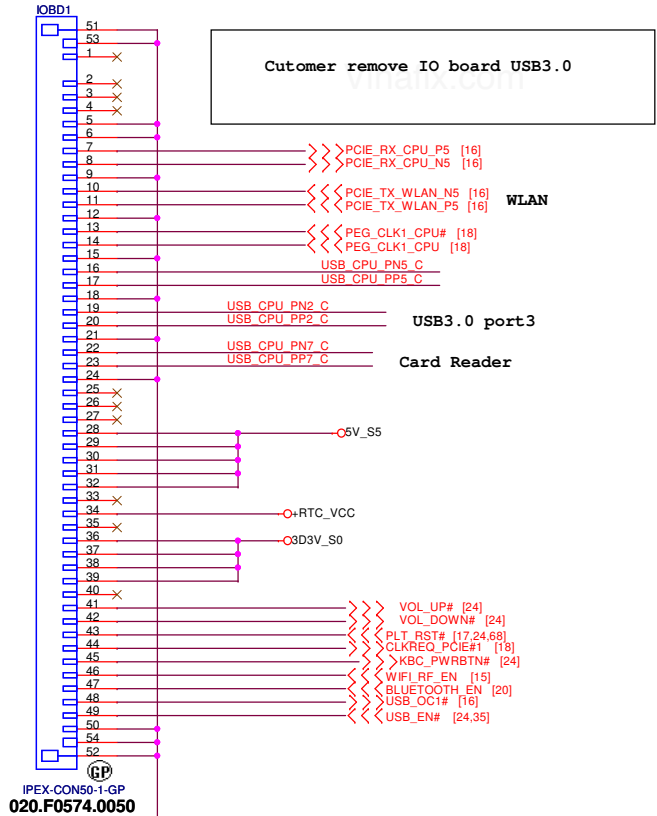
GPIO_TPAD: TBD
(Touch pad wake# for S3 wake up @ PCH GPIO??)

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

~~Need to check if it is Active High or Active Low
and check if there is PH on TPAD side.~~



Main Func = IO Connector



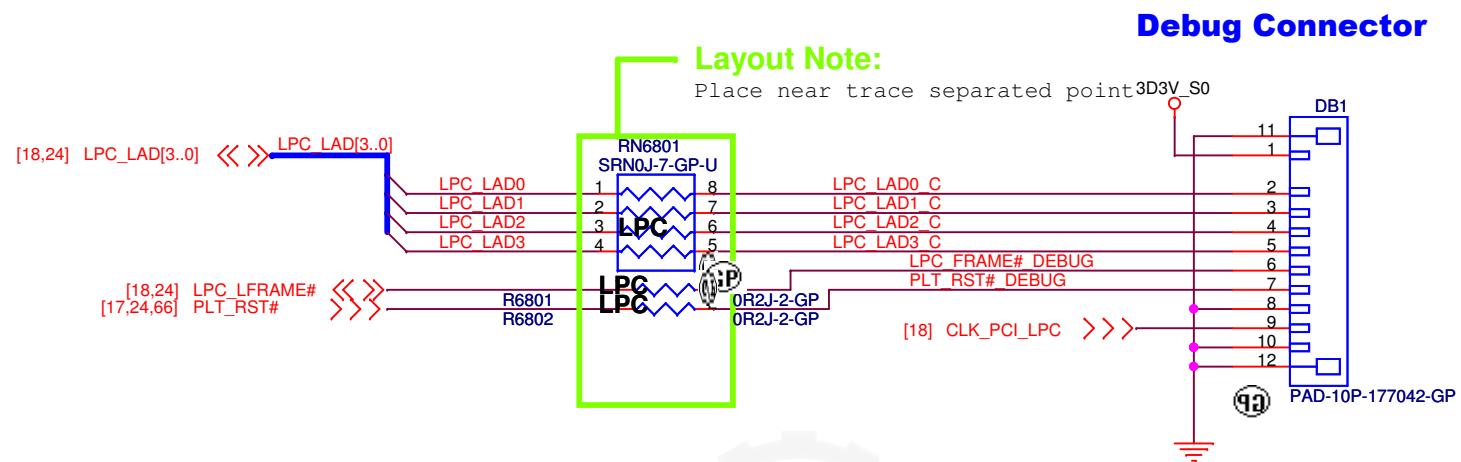
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Main Func = Debug

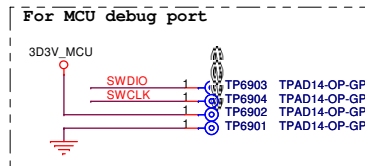
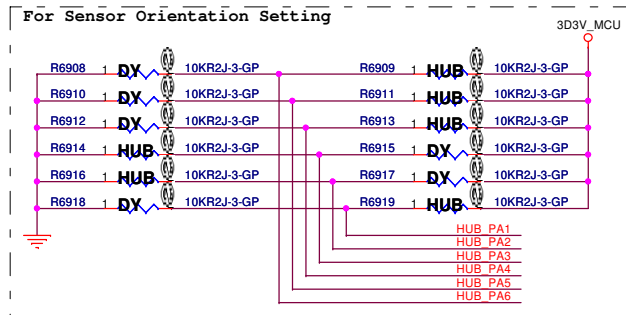
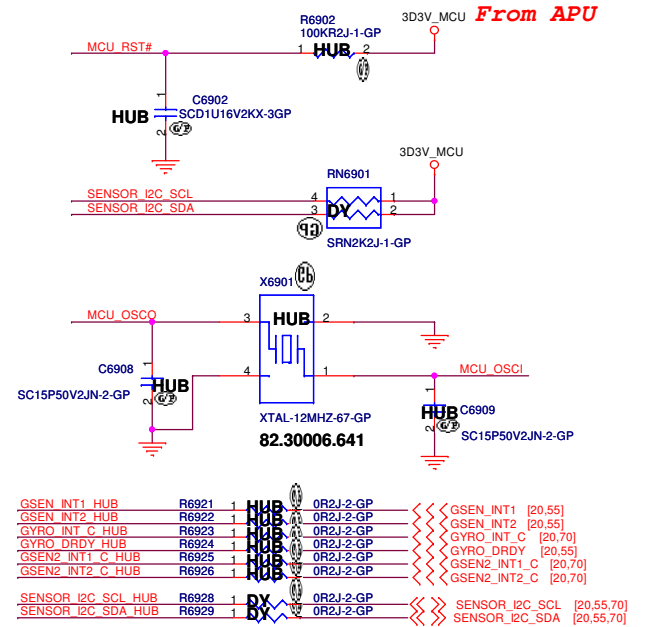
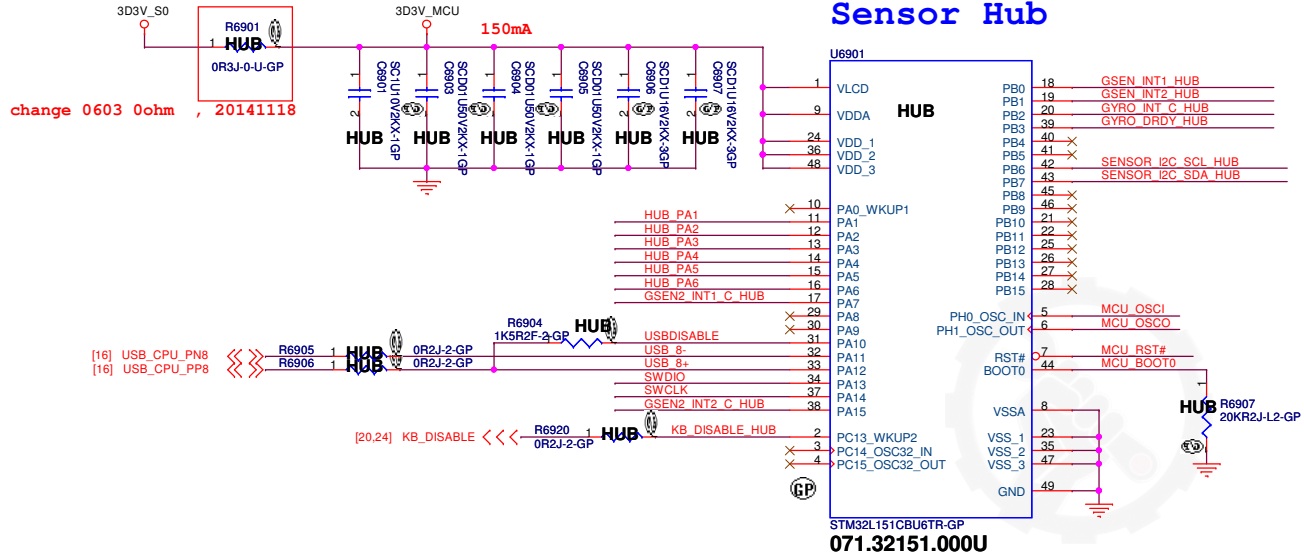
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20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

<Core Design>

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Dubug connector			
Size A4	Document Number Starload SKL-U		Rev A00
Date: Thursday, February 25, 2016		Sheet 68 of 106	



<Core Design>

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Title

Reserved

Size
A3

Document Number

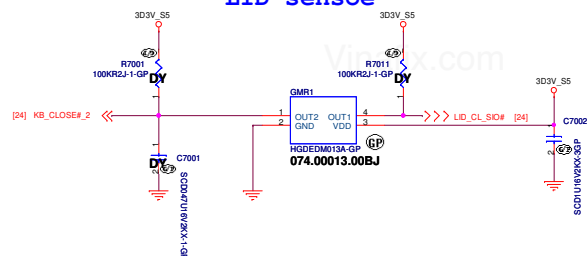
Starload SKL-U

Rev
A00

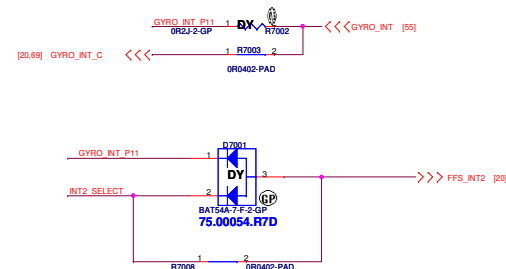
Date: Thursday, February 25, 2016

Sheet 69 of 106

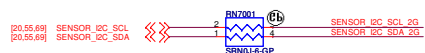
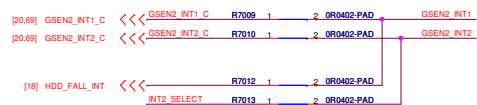
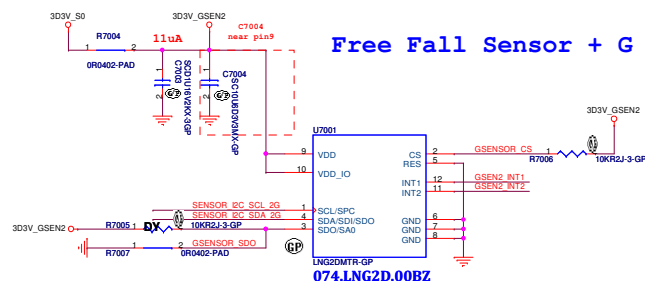
LID sensoe



combine G



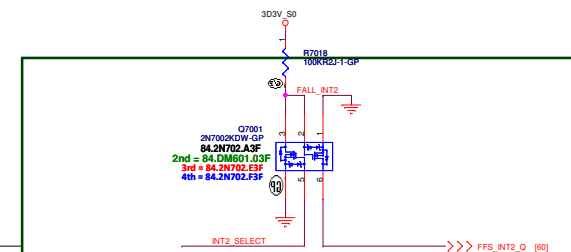
Free Fall Sensor + G Sensor



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U6602



Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

<Core Design>

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<Core Design>



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Title

RESERVED

Size
A3

Document Number

Starload SKL-U

Rev

A00


Date: Thursday, February 18, 2016

Sheet 71 of 106

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<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB3.0 PORT			
Size	Document Number		Rev
A3	Starload SKL-U		A00
Date:	Thursday, February 18, 2016		Sheet 72 of 106

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<Core Design>


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Title			
Reserved			
Size	Document Number		Rev
A3	Starload SKL-U		A00
Date: Thursday, February 18, 2016		Sheet 74 of 106	1

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Title

Size
A3

Document Number
Starload SKL-U

Date: Thursday, February 18, 2016

Reserved

Rev
A00

Sheet 75 of 106

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5
Main Func = dGPU

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Main Func = dGPU

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Title			GPU-VRAM1,2 (1/4)	
Size	Document Number		Rev	
A3			Starload SKL-U	
Date: Thursday, February 18, 2016		Sheet	81	of 106

D

C

B

A

Main Func = dGPU

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<Core Design>



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Title			GPU-VRAM3,4 (2/4)	
Size	Document Number		Rev	
A3			Starload SKL-U	
Date: Thursday, February 18, 2016		Sheet	82	of 106

D

C

B


A

Main Func = dGPU

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM5,6 (3/4)			
Size	Document Number		Rev
A3	Starload SKL-U		A00
Date:	Thursday, February 18, 2016		Sheet 83 of 106

Main Func = dGPU

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU-VRAM7,8 (4/4)			
Size	Document Number		Rev
A3	Starload SKL-U		A00
Date: Thursday, February 18, 2016		Sheet 84 of	106

Main Func = dGPU

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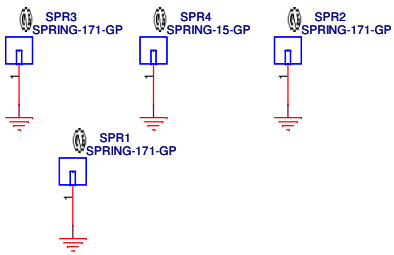


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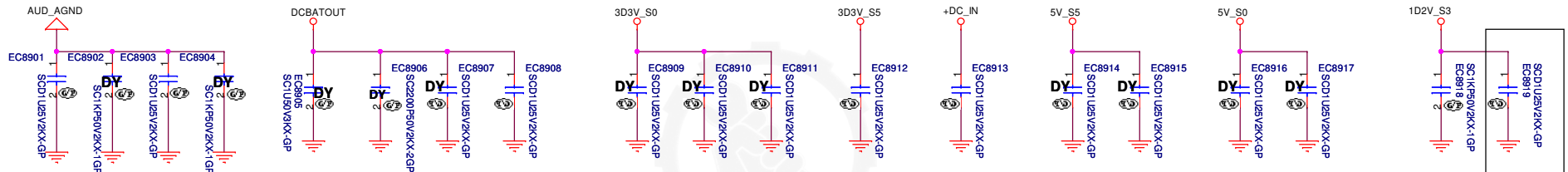
Main Func = UnusedParts

34.4YW18.001

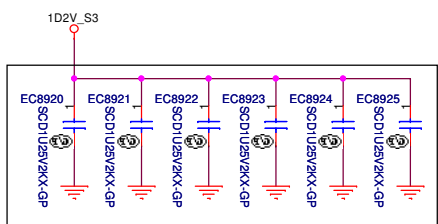


SSID = EMI

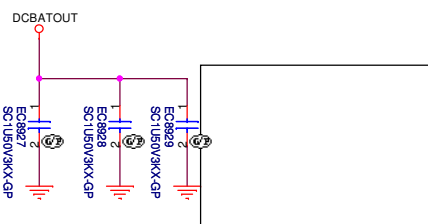
Mind the voltage rating of the caps.



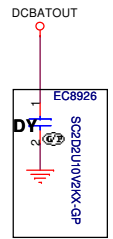
SSID = RF



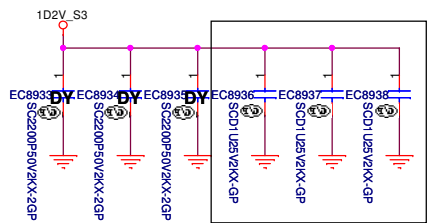
Change to 0.1uF at 20150427 for EMI



Remove EC8931,EC8932,EC8926,EC8930for placement




RF request 2016/01/12 modify



Change to 0.1uF at 20150427 for EMI

<Core Design>



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Title


UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A3	Starload SKL-U	A00
Date:	Thursday, February 18, 2016	Sheet 89 of 106

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<Core Design>



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Title

Size
A3

Document Number
Starload SKL-U

Date: Thursday, February 18, 2016

Rev
A00


Sheet 90 of 106

SSID = TPM

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Title			
TPM2.0			
Size	Document Number		Rev
A3	Starload SKL-U		A00
Date:	Thursday, February 18, 2016		Sheet 91 of 106

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)Finger Print			
Size A4	Document Number Starload SKL-U		Rev A00
Date: Thursday, February 18, 2016		Sheet 92 of	106



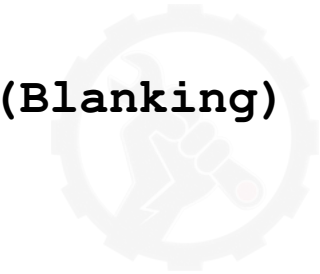
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A

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Size A3	Document Number Starload SKL-U	Rev A00
Date: Thursday, February 18, 2016	Sheet 97 of 106	

Size A3	Document Number Starload SKL-U	Rev A00
Date: Thursday, February 18, 2016	Sheet 97 of 106	

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<Core Design>



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Title

CRT Switch

Size

A3

Document Number

Starload SKL-U

Rev

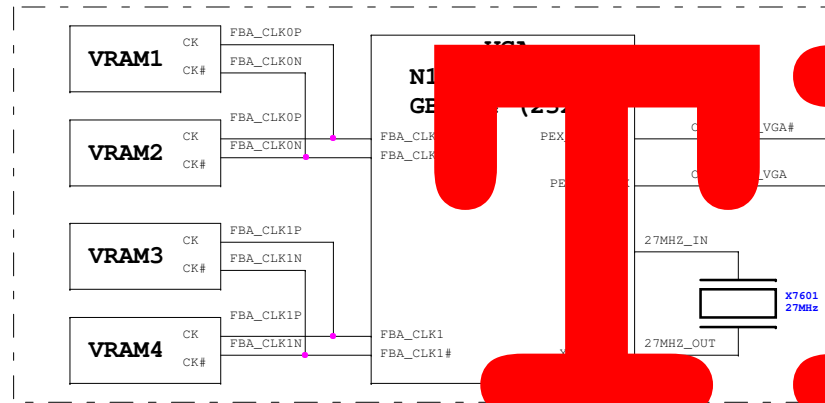
A00

Date: Thursday, February 18, 2016

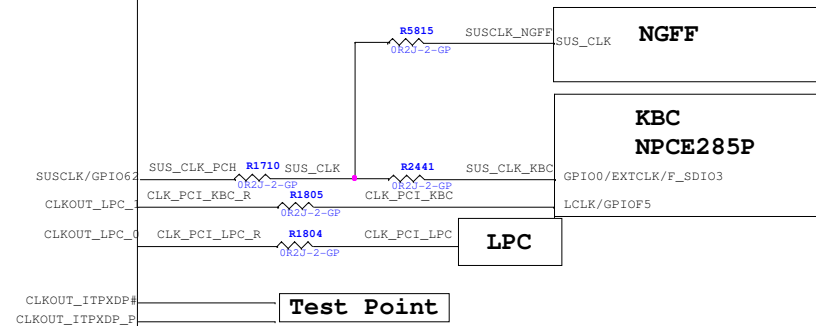
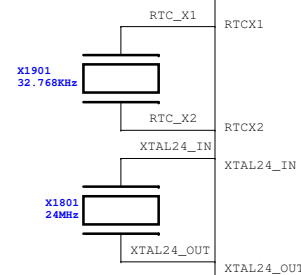
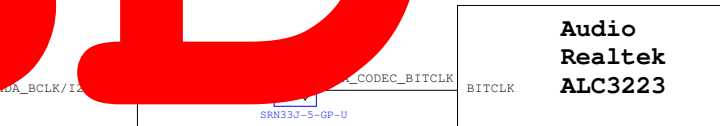
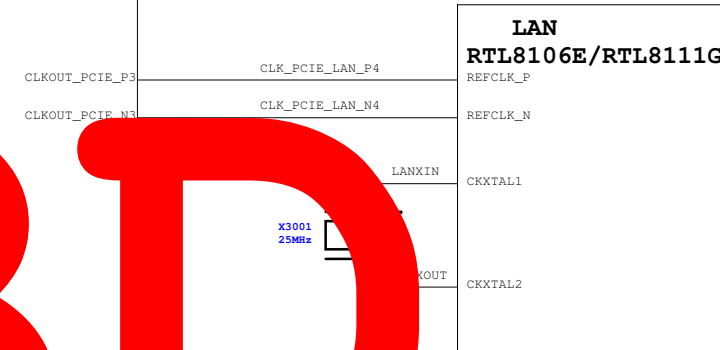
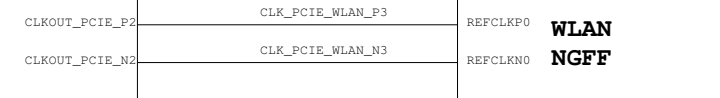
Sheet 98 of 106

DDR3L DIMM1

CK0	M_A_DIMA_CLK_DDR0	SA_CLK0
CK0#	M_A_DIMA_CLK_DDR0	SA_CLK#0
CK1	M_A_DIMA_CLK_DDR1	SA_CLK1
CK1#	M_A_DIMA_CLK_DDR1	SA_CLK#1



The image shows a hardware schematic diagram with a large red 'TBD' watermark. The schematic includes components like a 27MHz oscillator (X7601) and various signal lines. The text 'TBD' is prominently displayed in the center, indicating that the design is not yet finalized.



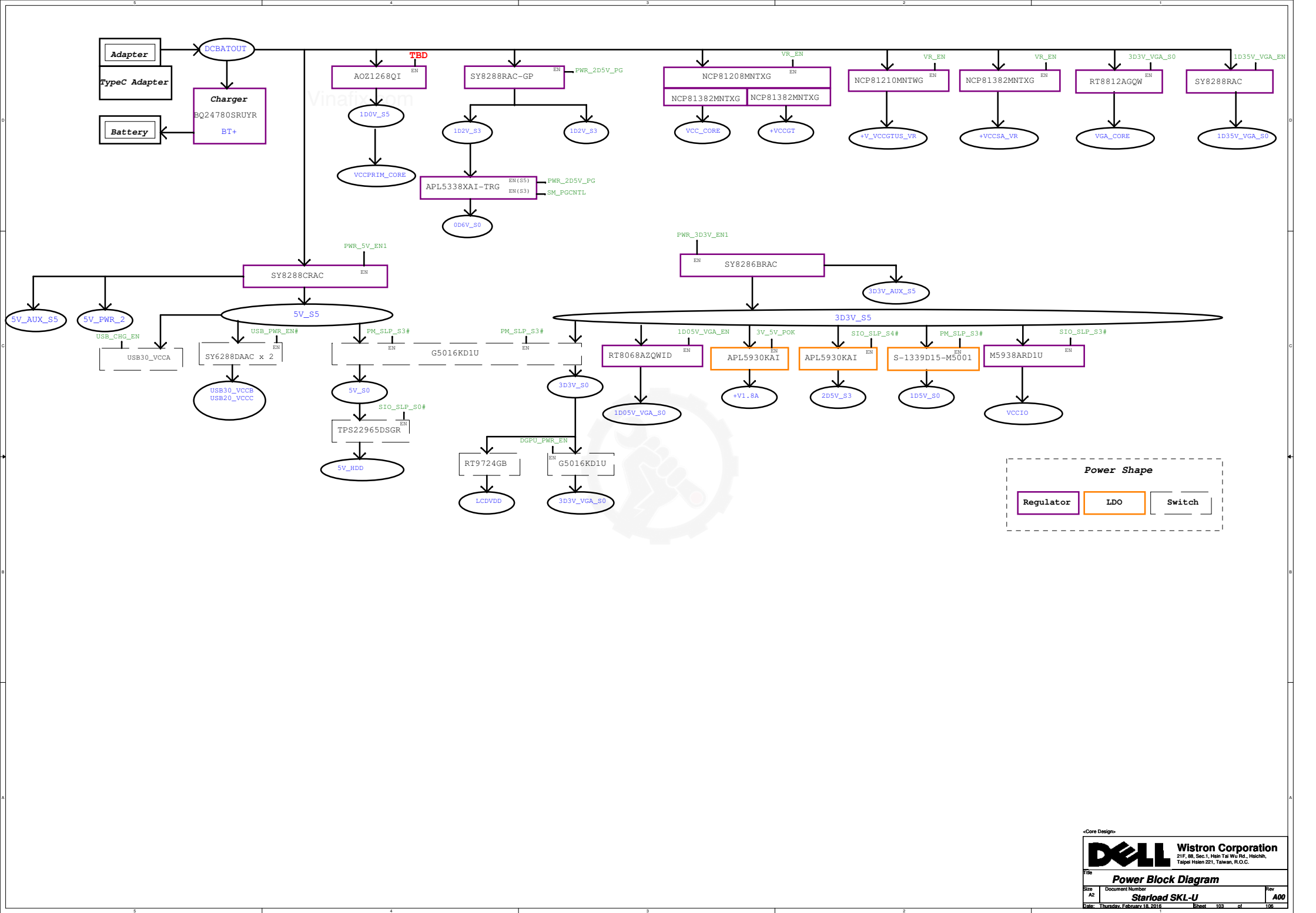
[illegible][illegible]

Title			
Change History			
Size A3	Document Number Starload SKL-U	Rev A00	
Date: Thursday, February 18, 2016	Sheet 101	of 106	

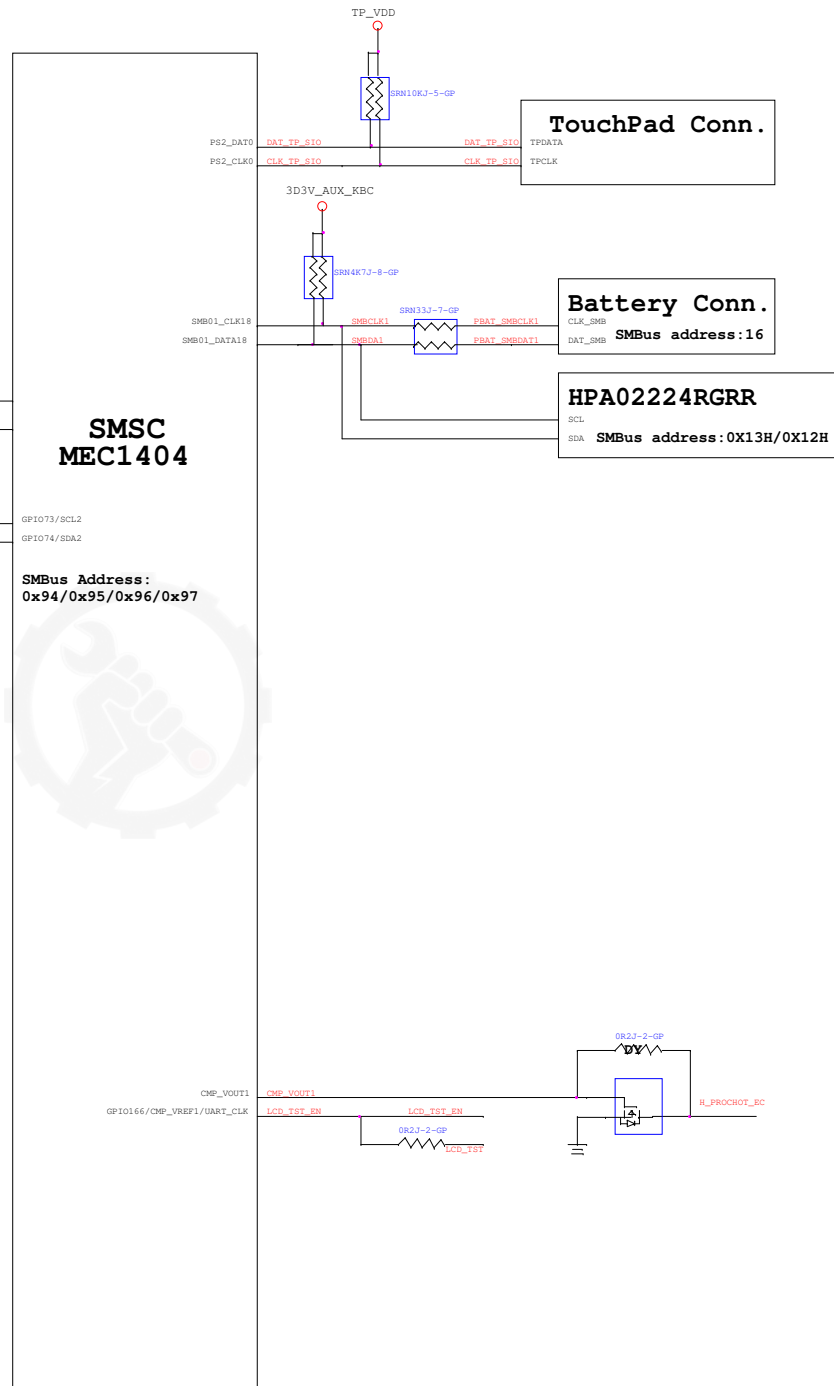
DELL Wistron Corporation
207, 2nd, Sec. 7, Zhongxing Rd., Hsinchu,
Taipei Hsien 307, Taiwan, R.O.C.

Power Sequence

Startled 037.11

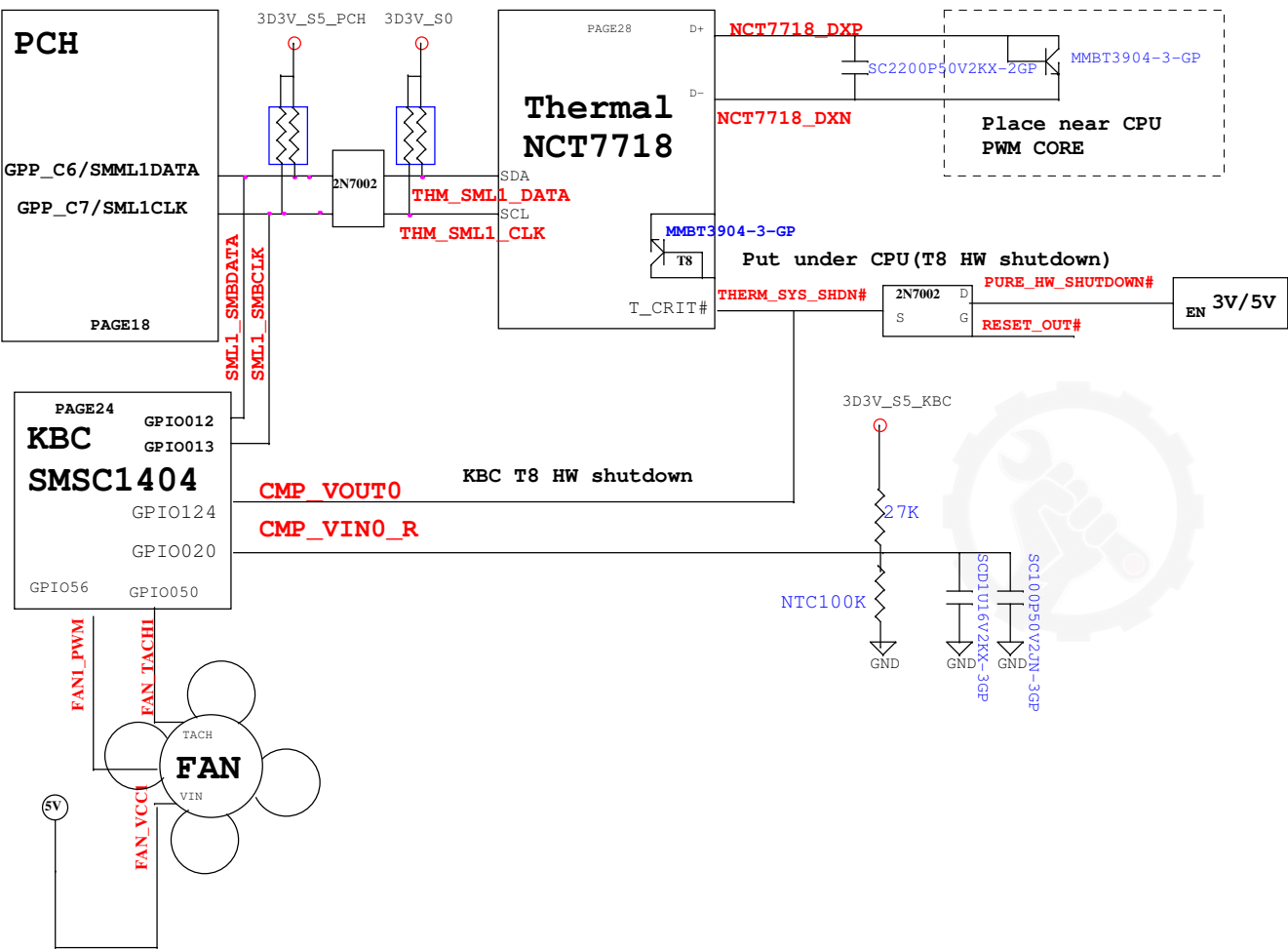


KBC SMBus Block Diagram

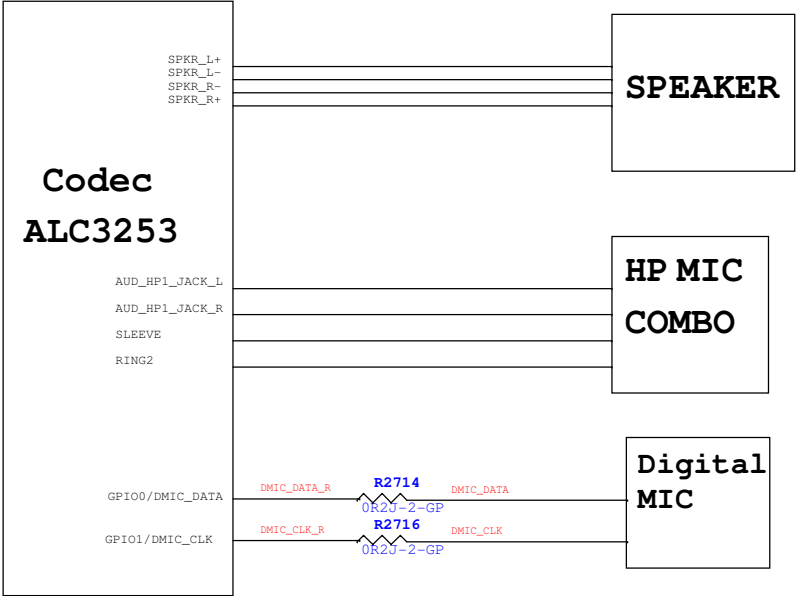


Thermal Block Diagram

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Audio Block Diagram



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<Core Design>

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Title		
<i>SIP connector</i>		
Size A	Document Number <i>Starload SKL-U</i>	Rev <i>A00</i>
Date: Thursday, February 18, 2016		Sheet 106 of 106